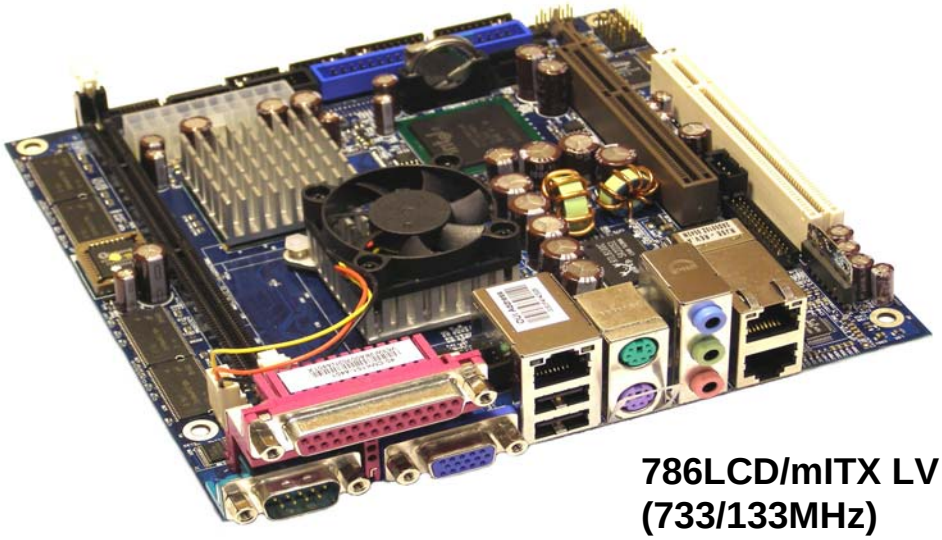
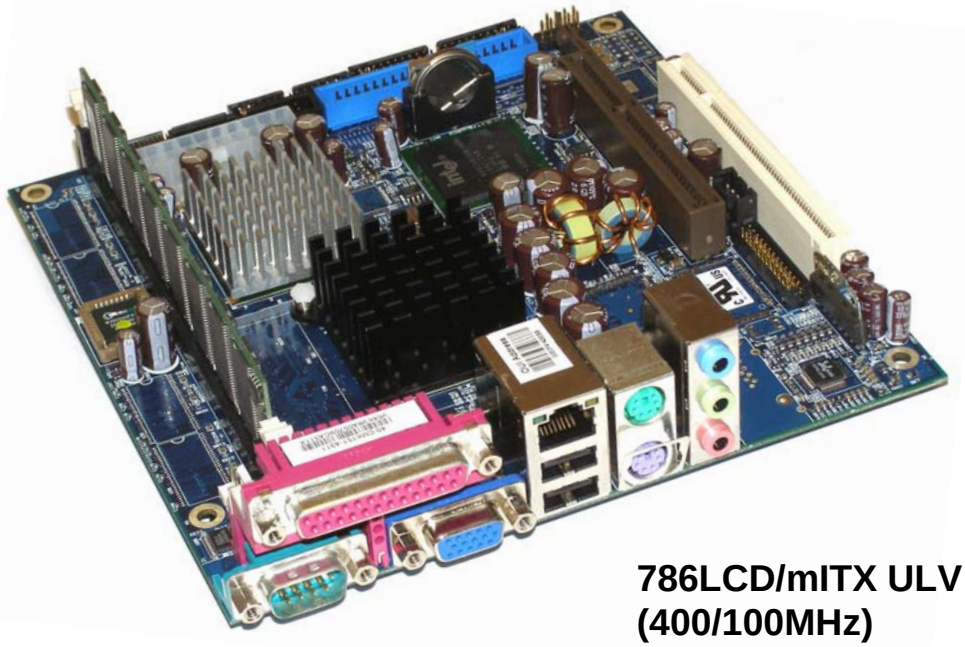
User Manual

for

786LCD/mITX family



786LCD/mITX LV
(733/133MHz)



786LCD/mITX ULV
(400/100MHz)

Document revision history.

Revision	Date	By	Comment
J	May 30th 2008	MLA	PME/WOL option added to BIOS. Battery type updated.
I	April 22nd 2008	MLA	Battery load information added.
H	Oct. 18th, 2007	MLA	Note on CDROM audio connector and on ETHER2/3 connector. Included warning in Installation procedure.
G	May 25th, 2007	MLA	USB0/3 pull-up resistor removed from description. USB description modified. Suspend LED /HDD LED info added.
F	Dec. 27th, 2006	MLA	USB port locations corrected. SATA and RAID installation guide added. Riser card PCI IRQ and INT info added. "Onboard connectors" updated. BIOS part updated. Other minor details corrected.
E	July 5th, 2006	MLA	BKLTCTL and FAN3OUT signal description corrected.
D	July 3rd, 2006	MLA	Pictures modified/added. Chapter 3.3 corrected, chapter Power Concumption included. Info on Boot Logo added. RTC Resume function Watchdog Support added. Added info to Fan Cruise Control.
C	April. 26th, 2006	MLA	Picture in Chapt. 4.1.1 changed. Feature Connector specifications corrected.
B	Mar. 17th, 2006	MLA	Page 12, 400MHz version has no onboard RAM. Sys Fan & CPU Fan location exchanged. USB4/5 has no Shroud. Audio connector pin 11/12 corrected to NC. Frontpanel connector pin 9 removed. Onboard Connector table updated. Chapter System Resources added. BIOS description added.
A	Feb 8th, 2006	MLA	COMA-D corrected and changed to Port1 -4. LVDS Display res.
0	Sept 6th, 2005	PJA	First preliminary manual version.

Life Support Policy

KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

KONTRON Technology Technical Support and Services

If you have questions about installing or using your KONTRON Technology Product, check this User's Manual first – you will find answers to most questions here. To obtain support, please contact your local Distributor or Field Application Engineer (FAE).

Before Contacting Support: Please be prepared to provide as much information as possible:

- CPU Board
  1. Type.
  2. Part-number (Number starting with "535").
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup in the Kontron Section).
  4. BIOS Settings different than *Default* Settings (Refer to the Software Manual).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

Table of contents:

1. Introduction

This manual describes the 786LCD/mITX board made by KONTRON Technology A/S. The boards will also be denoted 786LCD family if no differentiation is required.

All boards are to be used with the Intel® Celeron® LV and ULV Processors.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the 786 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. Except for the CMOS Clear jumper, no jumper configuration is required.

2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has SDRAM mounted. In this case Step 2 can be skipped.

1. Turn off the power supply.

2. Insert the SDRAM module (optional). Be careful to push it in the slot before locking the tabs. For a list of approved SDRAM modules contact your Distributor or FAE.
   PC133,168pin SDRAM modules are supported.

3. Insert all external cables for hard disk, keyboard etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to flat panel support. To achieve UDMA-66/100/133 performance on the IDE interface, 80poled UDMA cables **must** be used. If using the IDE_S2 connector care should be taken in correct orientation when attaching the female cable. The cables that KONTRON provide do not have a key. There is possibility of damage to the HDD or PCB if the cable is not orientated correctly.

Note: If the Audio Amplifier shall be used to generate up to 3W on the Audio ouput channels, then make sure that sufficent airflow is around the Audio Amplifier. The Amplifier has integrated Thermal Protection and will not be damaged even though the airflow is insufficient for normal operation.

4. Connect power supply to the board by the ATXPWR connector.

5. Turn on the power on the ATX power supply.

6. The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.

7. Enter the BIOS setup by pressing the “F2” key during boot up. Refer to the Software Manual (under preparation) for details on BIOS setup.
   Enter Advanced Menu / CPU Configuration / Intel SpeedStep Tech. and set this option to “Maximum Performance”.

Note: To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

2.2 Requirement according to EN60950

Users of 786LCD boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarises the features of the 786LCD/mITX embedded motherboard.

Form factor	786LCD/mITX: mini ITX (170.18millimeters by 170.18millimeters)
Processor	• Support for Intel Celeron LV and Celeron ULV Processors in mPGA478 socket with 400MHz system bus.
Memory	• Onboard 128MB or 256MB PC133 SDRAM mounted depending on configuration. • 1x168pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets. Support of up to 256MB memory modules. • Support for up to 512MB of system memory (onboard 256MB + 256MB in DIMM socket) • ECC support is not supported
Chipset	Intel 815E Chipset consisting of: • Intel 82815 Graphics and Memory Controller Hub(GMCH) • I/O Controller Hub (ICH or ICH2)
Video	• Intel Graphics controller • Analog Display Support, 230-MHz integrated 24-bit RAMDAC with support for analogue monitors up to 1600x1200x8bit at 85 Hz • DVI interface support (depending on configuration) • LVDS panel support, single or dual channel, 1280x1024 max. (1024x768 max. using 786LCD/mITX ULV), DOS, WinXP/XPe/2000/CE.NET • AGP 2.0, 1.5V connector (supporting 1x, 2x, and 4x AGP cards). • DVO on AGP connector not supported
Audio	Audio, AC97 version 2.3 subsystem using the Realtek ALC655 codec • Audio Amplifier: 2x3W • Line-out • CDROM in • SPDIF Interface • Microphone Onboard speaker
I/O Control	Winbond W83627THF LPC Bus I/O Controller
Peripheral interfaces	• Six USB 2.0 ports • Two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s, and 400M bits/s • Four Serial ports (RS232). • One Parallel port, SPP/EPP/ECP • Two Serial ATA 150 IDE interfaces • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66/100 support • PS/2 keyboard and mouse ports

(continued)

LAN Support	3x 10/100Mbits/s LAN subsystem using the Realtek RTL8100C LAN controllers **or** 1x 10/100Mbits/s LAN subsystem using the Realtek RTL8100C LAN controllers depending on board configuration. PXE and RPL netboot supported. Wake On LAN (WOL) supported.
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 1.0, 2.0), Plug and Play o Suspend To Ram o Suspend To Disk • SW Watchdog and RTC Resume supported by BIOS 0.7 an above • Secure CMOS/ OEM Setup Defaults • "Always On" BIOS power setting • Boot Logo is optional (640x480, 24bit color) in customer specific BIOS
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support
Expansion Capabilities	• SMBus routed to FEATURE connector • LPC Bus routed to LPC connector • DDC Bus routed to LVDS connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector • PCI Bus routed to PCI slot (PCI Local Bus Specification Revision 2.2)
Hardware Monitor Subsystem	• Fan control system for three onboard Fan control connectors: CPU FAN, SYSTEM FAN and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. • Voltage monitoring • Intrusion detect input • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• Win2000 • WinXP • Win98 (LVDS Display not supported) • Win2003(LVDS Display not supported) • WinXP Embedded (limitations may apply) • WinCE.net (limitations may apply) • Linux: Feodora Core 3, Suse 9.2 (limitations may apply)

(continued)

Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 199,799hours (22,8years) , Calculation based on Telcordia SR-332 method. **Restriction of Hazardeous Substances (RoHS):** The 786LCD-M family is planned for RoHS compliance. **Capacitor utilization:** No Tantal capacitors on board Only Japanese brand Aluminium capacitors rated for 100degrees Celsius used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / PN CR2032NL/LE or CR-2032L/BE. Approximately 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 6.2µA (no PSU connected). **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 Configuration overview

Feature	810045-4500, 786LCD/mITX LV Plus	810046-4500, 786LCD/mITX ULV Standard
CPU	Intel Celeron LV 733MHz	Intel Celeron ULV 400 MHz
Onboard Memory	256MB SDRAM, PC133	No
CRT	Yes	Yes
LVDS	Yes (Max. 1280x1024)	Yes (Max. 1024x768)
DVI	No	No
LAN	3x10/100MBit	1x10/100MBit
IEEE1394	2xIEEE1394	No
PATA	Yes	Yes
SATA	Yes	No
Compact Flash	Yes	Yes
Audio	Yes	Yes
USB	Yes, 6xUSB2.0	Yes, 6xUSB2.0
Serial Ports	Yes, 4xRS232	Yes, 4xRS232
Parallel Port	Yes	Yes
PS/2 / KBD	Yes	Yes
PCI	Yes	Yes
AGP	Yes	Yes

Table is preliminary and subject to change without notification

3.3 System Memory support

The 786LCD/mITX board has one onboard DIMM sockets and optionally on board memory.

- Maximum total 512MB
- 64-bit data interface
- ECC not supported

The onboard memory is:

- 0 MB (786LCD/mITX ULV Standard)
- 256 MB/ PC133 (786LCD/mITX LV Plus)

The socket memory can be:

- 168-pin PC100/PC133 SDRAM DIMMs from 32 MB to 256 MB
- Single - or double sided DIMMs with gold-plated contacts.

Note: 786LCD/mITX ULV Standard running PC100 even PC133 is installed.

3.4 Power consumption

The following power consumptions is based on measurements and are typical values.
The Power consumption of Keyboard and Mouse are included and CRT, HD and Floppy are not included.

786LCD/mITX LV Plus (733MHz/PC133)

In Windows XP and running 3DMARK2000:

Supply	Current draw	Power consumption
+3V3	3.2A	10.5 W
+5V	1.5A	7.5 W
+12V	333mA	4.0 W
+5VSB	160mA	0.8 W
Total power consumption		22.8 W

In Windows XP idle, total power consumption is 19 W.
In Standby (S3) power consumption (+5VSB) is 1.2 W.

786LCD/mITX ULV Standard (400MHz/PC100)

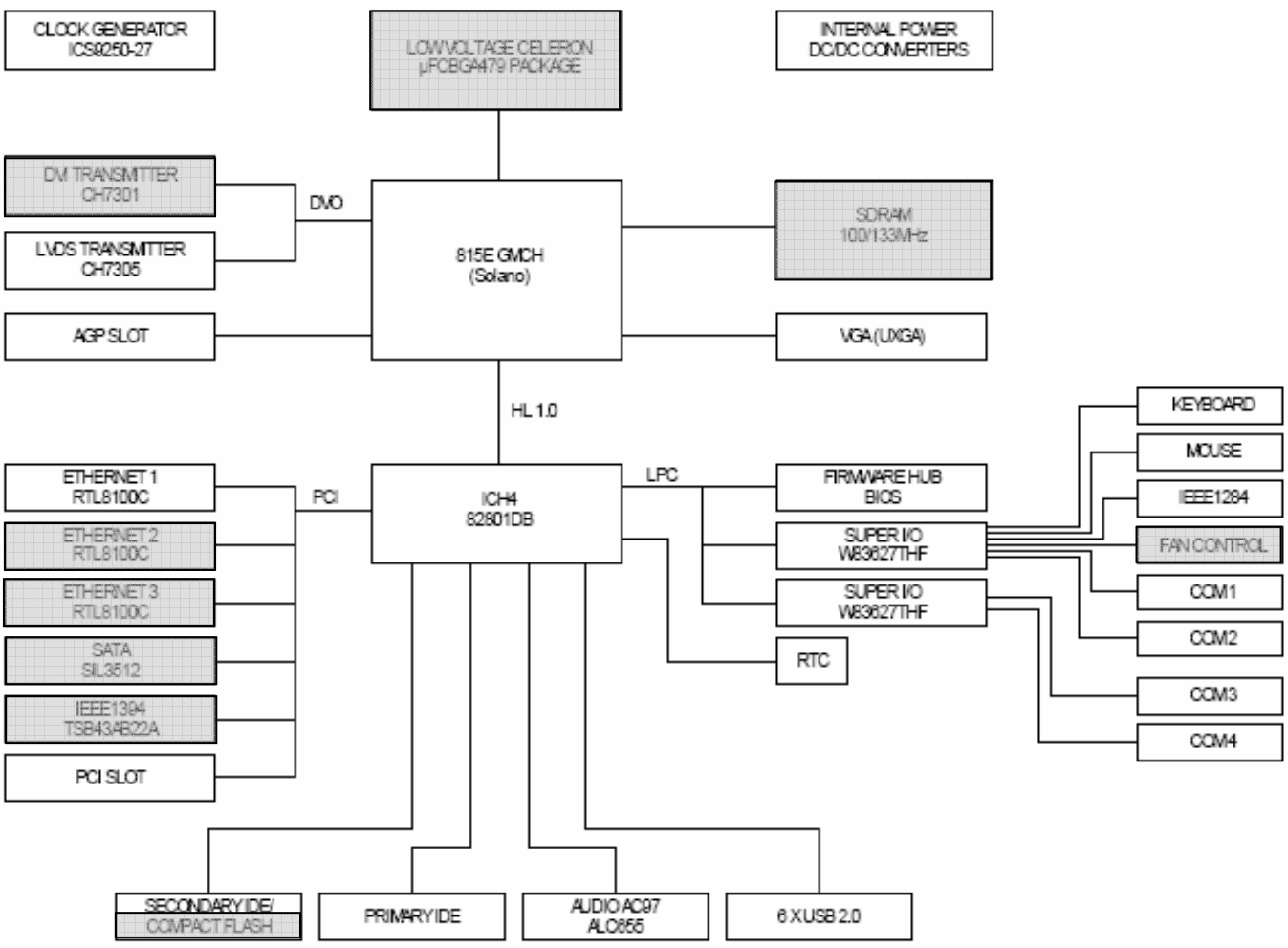
In Windows XP 3DMARK2000:

Supply	Current draw	Power consumption
+3V3	2.4A	8.0 Watt
+5V	920mA	4.6 Watt
+12V	210mA	2.5 Watt
+5VSB	145mA	0.7 Watt
Total power consumption		15.8 Watt

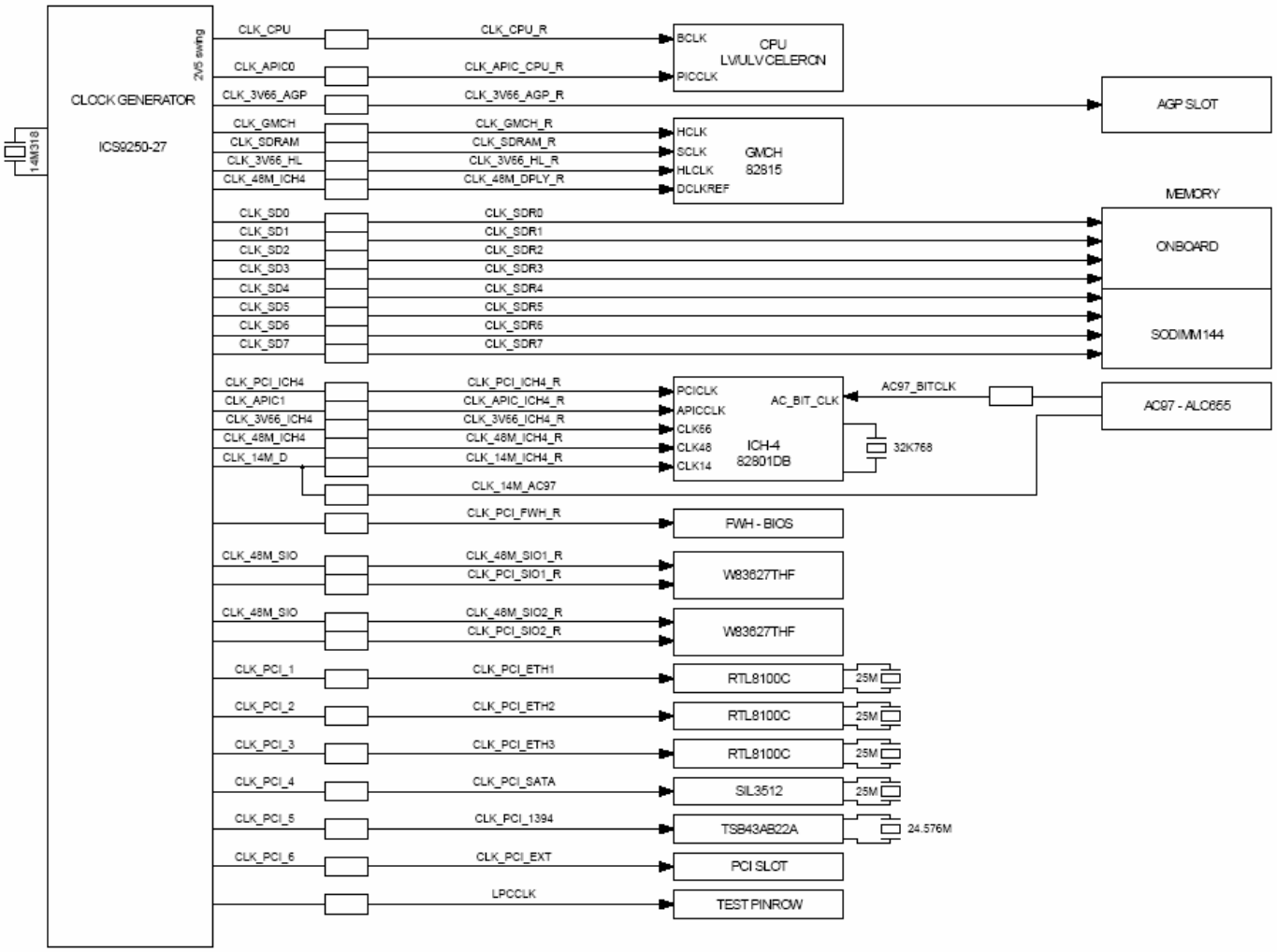
In Windows XP idle, total power consumption is 13 W.
In Standby (S3) power consumption (+5VSB) is 1.1 W.

3.5 System overview

The block diagram below shows the architecture and main components of the 786LCD boards. The two key components on the board are the Intel® 815E and Intel® ICH4 Embedded Chipsets.
Components shown shaded may differ depending on variants of the board.



3.6 786LCD Clock Distribution



4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

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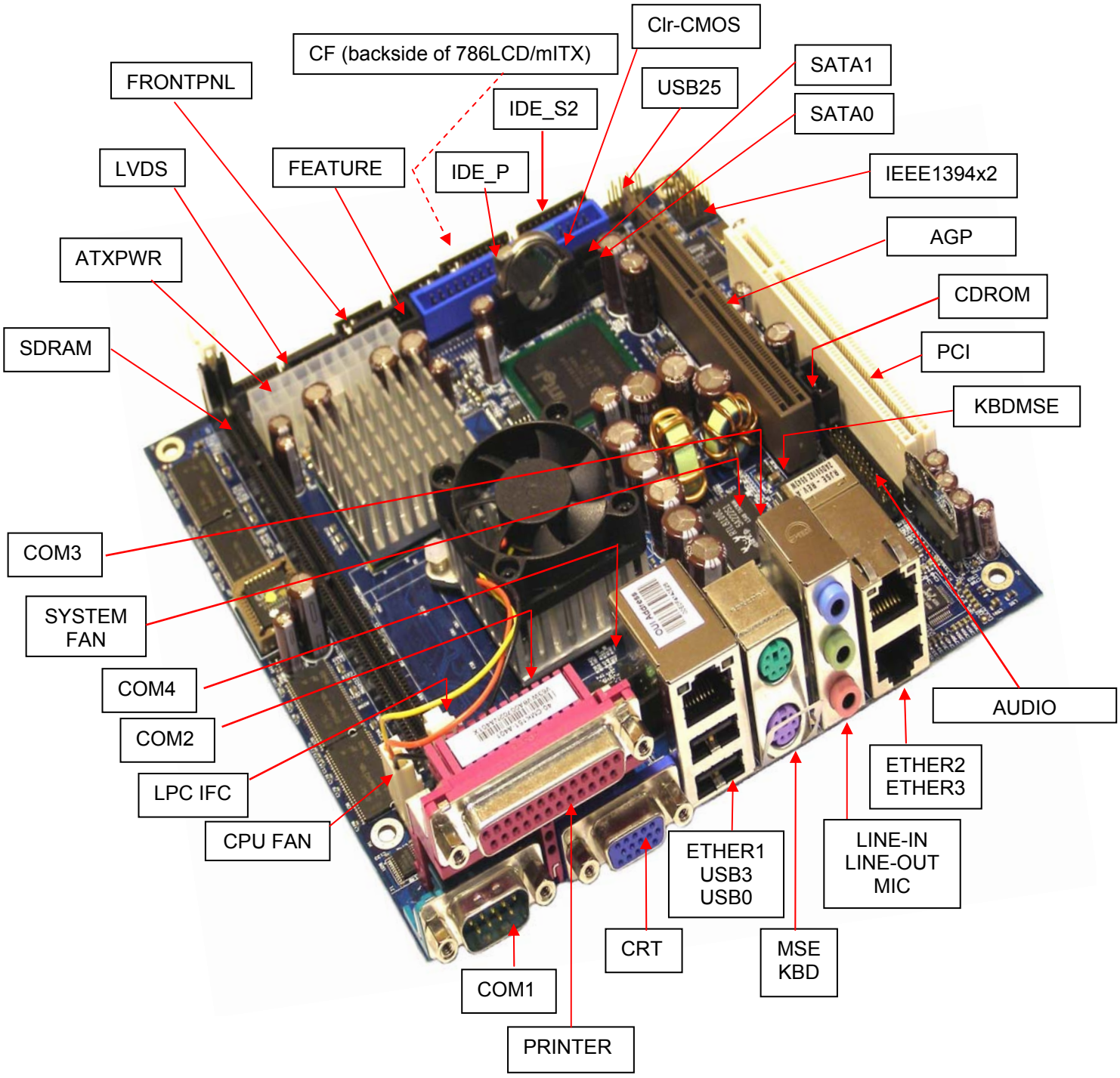
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

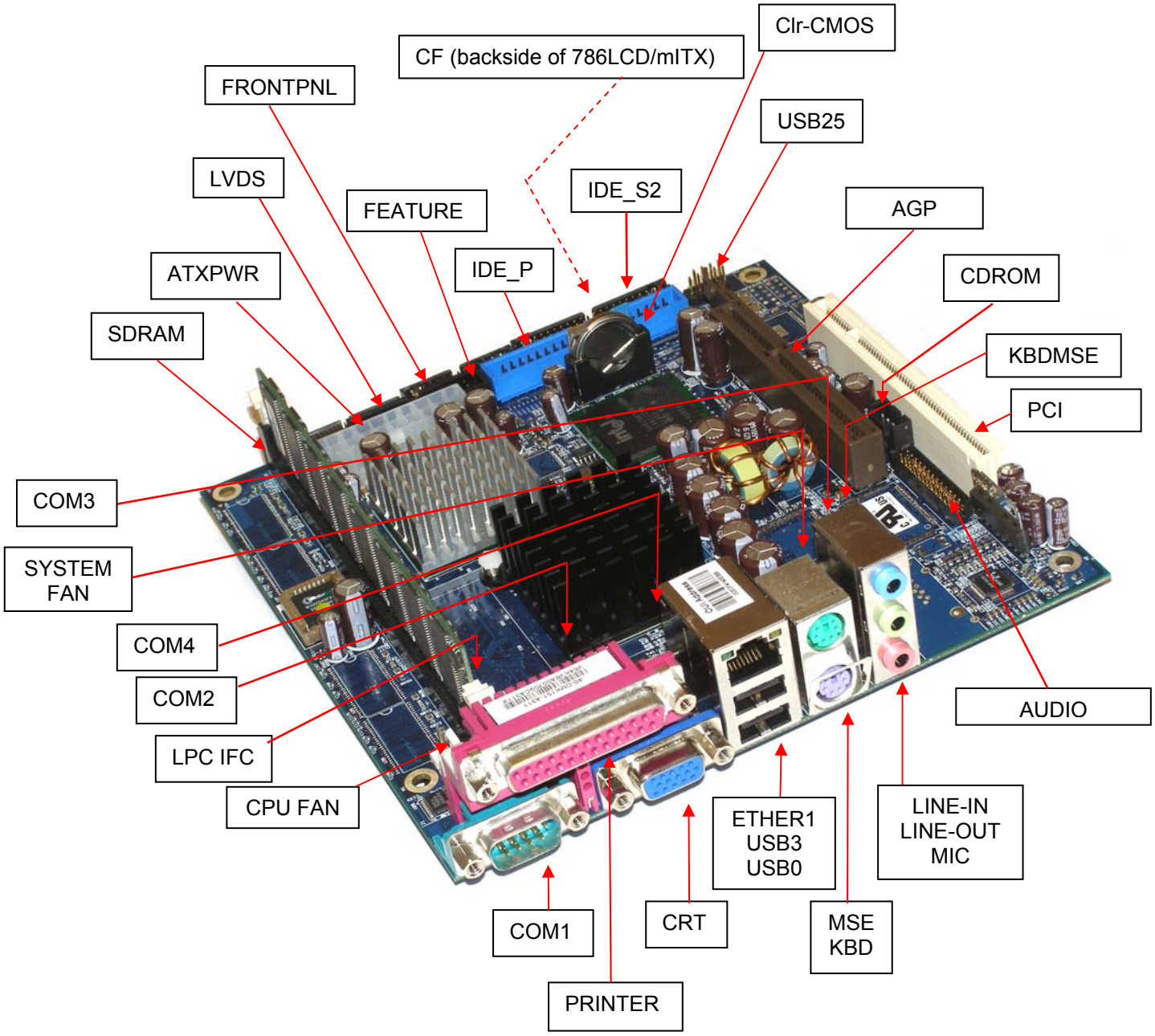
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

4.1.1 786LCD/mITX LV Plus



4.1.2 786LCD/mITX ULV Standard



4.2 Power Connector (ATXPWR)

The 786LCD/mITX is designed to be supplied from a standard ATX power supply.

Power Connector 786LCD/mITX

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	+12V	10	20	5V	PWR	-	-	
	-	-	PWR	SB5V	9	19	5V	PWR	-	-	
	4K7	-	I	P_OK	8	18	-5V	PWR	-	-	1
	-	-	PWR	GND	7	17	GND	PWR	-	-	
	-	-	PWR	5V	6	16	GND	PWR	-	-	
	-	-	PWR	GND	5	15	GND	PWR	-	-	
	-	-	PWR	5V	4	14	PSON#	OC	-	-	
	-	-	PWR	GND	3	13	GND	PWR	-	-	
	-	-	PWR	3V3	2	12	-12V	PWR	-	-	
	-	-	PWR	3V3	1	11	3V3	PWR	-	-	

Note: -5V supply is not used onboard.

The requirements to the supply voltages are as follows (also refer to ATX specification):

Supply	Min	Max	Tolerance
3V3	3.14V	3.46V	+/-5%
5V	4.75V	5.25V	+/-5%
SB5V	4.75V	5.25V	+/-5%
+12V	11.4V	12.6V	+/-5%
–12V	–13.2V	–10.8V	+/-10%

Control signal description:

Signal	Description
P_OK	Active high signal from the power supply indicating that the 5V and 3V3 supplies are within operating limits. It is strongly recommended to use an ATX supply with the 786LCD/mITX boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the 786LCD/mITX boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from 5V_STB when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	4K7	
			-	NC	6 5	KBDCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	4K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

4.4 Display Connectors

The 786LCD board family provides onboard two basic types of interfaces to a display: Analog CRT interface and a digital interface available as either LVDS dual channel interface or DVI (analogue/ digital) depending on the board configuration. Further an onboard AGP slot supports AGP 2.0 including 4X AGP data transfers. DVO is not supported in the AGP connector.

4.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	560R	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	560R	

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

4.4.2 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Pin		Signal	Type	Note
	PWR	+12V	1	2	+12V	PWR	
	PWR	+12V	3	4	+12V	PWR	
	PWR	+12V	5	6	GND	PWR	
	PWR	+5V	7	8	GND	PWR	
	PWR	LCDVCC	9	10	LCDVCC	PWR	
4K7Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	4K7Ω, 3.3V
4.7V level	AO	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
	PWR	GND	27	28	GND	PWR	
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
	PWR	GND	39	40	GND	PWR	

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM (high impedanse) output signal to implement voltage in the range 0-4.7V in steps of 0.3V. This signal is shared with the FAN3OUT signal (available in Feature Connector).
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API is available to operate the FAN3OUT (BKLTCTL) signal. Please notice that some Inverters has a limited voltage range 0- 2.5V and if voltage is > 2.5V the Inverter might latch up. In this case it is recommended to used a circuit to make sure the maximum voltage is not exceeded.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.

4.4.3 DVI Interface Connector (DVI IFC)

DVI functionality is not supported on actual 786LCD/mITX versions therefore the DVI IFC connector is not mounted.

Note	Type	Signal	Pin		Signal	Type	Note
		NC	1	2	NC		
		NC	3	4	NC		
		NC	5	6	GND	PWR	
	PWR	+5V	7	8	GND	PWR	
		NC	9	10	NC		
		LCDCK	11	12	LCDDA		
		NC	13	14	NC		
		HPDET	15	16	GND	PWR	
		TDC0	17	18	TDC0#		
		TDC1	19	20	TDC1#		
		TDC2	21	22	TDC2#		
		TLC	23	24	TLC#		
	PWR	GND	25	26	GND	PWR	
	PWR	GND	27	28	GND	PWR	
		RED	29	30	GND	PWR	
		GREEN	31	32	GND	PWR	
		BLUE	33	34	GND	PWR	
		VSYNC	35	36	HSYNC		
	PWR	GND	37	38	GND	PWR	
	PWR	GND	39	40	GND	PWR	

Signal Description – DVI Interface Connector:

Signal	Description
TDC0 TDC0#	DVI Data Channel 0 Outputs
TDC1 TDC1#	DVI Data Channel 0 Outputs
TDC2 TDC2#	DVI Data Channel 0 Outputs
TLC TLC#	DVI Clock Outputs
RED	RED component of RGB signal
GREEN	GREEN component of RGB signal
BLUE	BLUE component of RGB signal
HPDET	DVI Hot Plug Detect
LCDCK	Serial Channel Clock
LCDDA	Serial Channel Data

4.4.4 AGP connector - TBD

Note	Type	Signal	PIN		Signal	Type	Note
		OVRCNT	B1	A1	+12V	PWR	
	PWR	+5V	B2	A2	TYPEDET		
	PWR	+5V	B3	A3	RSVD		
		USB+	B4	A4	USB-		
	PWR	GND	B5	A5	GND	PWR	
		INTB	B6	A6	INTA		
		AGPCLK	B7	A7	RST-		
		GREQ	B8	A8	GGNT		
	PWR	+3.3V	B9	A9	+3.3V	PWR	
		ST0	B10	A10	**ST1**		
		ST2	B11	A11	RSVD		
	I	**RBF**	B12	A12	**PIPE**	I	
	PWR	GND	B13	A13	GND	PWR	
		RSVD	B14	A14	**WBF**	I	
	I	**SBA(0)**	B15	A15	**SBA(1)**	I	
	PWR	+3.3V	B16	A16	+3.3V	PWR	
	I	**SBA(2)**	B17	A17	**SBA(3)**	I	
	I	ADD_RS	B18	A18	ADD_RS		
	PWR	GND	B19	A19	GND	PWR	
	I	**SBA(4)**	B20	A20	**SBA(5)**	I	
	I	**SBA(6)**	B21	A21	**SBA(7)**	I	
		RSVD	B22	A22	RSVD		
	PWR	GND	B23	A23	GND	PWR	
	PWR	3V3AUX	B24	A24	RSVD		
	PWR	+3.3V	B25	A25	+3.3V	PWR	
			B26	A26			
			B27	A27			
	PWR	+3.3V	B28	A28	+3.3V	PWR	
			B29	A29			
			B30	A30			
	PWR	GND	B31	A31	GND	PWR	
			B32	A32			
			B33	A33			
	PWR	+1.5V	B34	A34	+1.5V	PWR	
			B35	A35			
			B36	A36			
	PWR	GND	B37	A37	GND	PWR	
			B38	A38			
		ADD_RS	B39	A39			
	PWR	+1.5V	B40	A40	+1.5V	PWR	
		M_I2CClk	B41	A41	M_DVI_Data		
		M_I2CData	B46	A46	M_DVI_Clk		
	PWR	+1.5V	B47	A47	M_DDCData		
		GPERR	B48	A48	PME		
	PWR	GND	B49	A49	GND	PWR	
		GSERR	B50	A50			
			B51	A51	M_DDCClk		
	PWR	+1.5V	B52	A52	+1.5V	PWR	
			B53	A53			
			B54	A54			
	PWR	GND	B55	A55	GND	PWR	
			B56	A56			
			B57	A57			
	PWR	+1.5V	B58	A58	+1.5V	PWR	
			B59	A59			
			B60	A60			
	PWR	GND	B61	A61	GND	PWR	
			B62	A62			
			B63	A63			
	PWR	+1.5V	B64	A64	+1.5V	PWR	
			B65	A65			
		VREFCG	B66	A66	VREFGC		

The AGP buffers operate only in 1.5V mode (not 3.3-V tolerant). The AGP interface supports 1x/2x/4x AGP signaling and 2x/4x Fast Writes.

Signal Description – AGP Connector:

Signal	Description
Address	
PIPE#	**Pipeline.** **During PIPE# Operation.** This signal is asserted by the AGP master to indicate a full-width address is to be enqueued on by the target using the AD bus. One address is placed in the AGP request queue on each rising clock edge while PIPE# is asserted. **During SBA Operation.** This signal is not used if SBA (Side Band Addressing) is selected. **During FRAME# Operation.** Not used.
SBA[7:0]	**Side-band Addressing.** **During PIPE# Operation.** Not used. **During SBA Operation.** These signals (the SBA, or side-band addressing, bus) are used by the AGP master (graphics component) to place addresses into the AGP request queue. The SBA bus and AD bus operate independently. That is, transactions can proceed on the SBA bus and the AD bus simultaneously. **During FRAME# Operation.** Not used.
Flow control	
RBF#	**Read Buffer Full.** **During PIPE# and SBA Operation.** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When R**BF#** is asserted the GMCH is not allowed to initiate the return low priority read data. That is, the GMCH can finish returning the data for the request currently being serviced, however it cannot begin returning data for the next request. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data, then it is not required to implement this signal. **During FRAME# Operation.** This signal is not used during AGP FRAME# operation.
WBF#	**Write-Buffer Full.** **During PIPE# and SBA Operation.** Write buffer full indicates if the master is ready to accept Fast Write data from the GMCH. When W**BF#** is asserted the GMCH is not allowed to drive Fast Write data to the AGP master. WBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data, then it is not required to implement this signal. **During FRAME# Operation**: This signal is not used during AGP FRAME# operation.
AGP Status	
ST[2:0]	**Status Bus.** **During PIPE# and SBA Operation.** Provides information from the arbiter to an AGP Master on what it may do. ST[2:0] only have meaning to the master when its GNT# is asserted. When GNT# is deasserted, these signals have no meaning and must be ignored. Refer to the AGP Interface Specification revision 2.0 for further explanation of the ST[2:0] values and their meanings. **During FRAME# Operation.** These signals are not used during FRAME# based operation; except that a '111' indicates that the master may begin a FRAME# transaction.
AGP Strobes	
ADSTB[0]	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
ADSTB#[0]	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
ADSTB[1]	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
ADSTB#[1]	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
SBSTB	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
SBSTB#	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.
AGP/PCI Signals-Semantics	
FRAME#	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes.

	During FRAME# Operation: G_FRAME# is an output when the GMCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH samples FRAME# active.
IRDY#	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#- based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.
TRDY#	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH acts as an AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
STOP#	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH acts as a FRAME#-based AGP initiator and is an output when the GMCH acts as a FRAME#- based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
DEVSEL#	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
REQ#	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.
GNT#	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
AD[31:0]	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.

(continued)

CBE#[3:0]	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. The command encoding used during PIPE#- based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
PAR	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.
Hub Interface signals	
HL[10:0]	**Packet Data:** Data signals used for HI read and write operations.
HLSTB	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.
Clocks	
CLKIN	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/Hub interface.
DPMS	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during S1-M and needs to be 1.5 V. So, an example would be to use a 1.5-V version of SUSCLK from ICH4-M.

4.5 Parallel ATA harddisk interface

Two parallel ATA harddisk controllers are available on the board – a primary and a secondary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller board by means of the 40 pin IDC connectors, IDE_P.
The secondary controller is shared between the IDE_S2 connector (which is intended for 2½" harddisks) and the backside Compact Flash connector.
The harddisk controllers support Bus master IDE, ultra DMA 33/66/100MHz and standard operation modes. Ultra DMA mode is the fastest with up to 100 MB/Sec bandwidth, to utilize this mode a special driver is required (see Software Manual).

The signals used for the harddisk interface are the following:

Signal	Description
DA*2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS*1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D*15..8	High part of data bus.
D*7..0	Low part of data bus.
IOR*#	I/O Read.
IOW*#	I/O Write.
IORDY*#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET*#	Reset signal to the hard disk. The signal is similar to RSTDRV in the PC-AT bus.
HDIRQ*	Interrupt line from hard disk. Routed by the SiS630 chipset to PC-AT bus interrupt.
CBLID*	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQ*	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK*#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT*#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
"*" is "A" for primary and "B" for secondary controller.
The pinout of the connectors are defined in the following sections.

4.5.1 IDE Hard Disk Connector (IDE_P)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETA#	1	2	GND	PWR	-	-	
	/10K	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	/5K6	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	1K	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	/10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.5.2 IDE Hard Disk Connector (IDE_S2)

This connector (44-pin 2.0 mm pitch) can be used for connection of up to two secondary IDE drives, but only if no drive(s) is installed via IDE_S2 socket.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETB#	1	2	GND	PWR	-	-	
	/10K	TBD	IO	DB7	3	4	DB8	IO	TBD	-	
	-	TBD	IO	DB6	5	6	DB9	IO	TBD	-	
	-	TBD	IO	DB5	7	8	DB10	IO	TBD	-	
	-	TBD	IO	DB4	9	10	DB11	IO	TBD	-	
	-	TBD	IO	DB3	11	12	DB12	IO	TBD	-	
	-	TBD	IO	DB2	13	14	DB13	IO	TBD	-	
	-	TBD	IO	DB1	15	16	DB14	IO	TBD	-	
	-	TBD	IO	DB0	17	18	DB15	IO	TBD	-	
	-	-	PWR	GND	19	20	NC	-	-	-	
	/5K6	-	I	DDRQB	21	22	GND	PWR	-	-	
	-	TBD	O	IOWB#	23	24	GND	PWR	-	-	
	-	TBD	O	IORB#	25	26	GND	PWR	-	-	
	1K	-	I	IORDYB	27	28	GND	PWR	-	-	
	-	-	O	DDACKB#	29	30	GND	PWR	-	-	
	/10K	-	I	HDIRQB	31	32	NC	-	-	-	
	-	TBD	O	DAB1	33	34	CBLIDB#	I			
	-	TBD	O	DAB0	35	36	DAB2	O	TBD	-	
	-	TBD	O	HDCSB0#	37	38	HDCSB1#	O	TBD	-	
	-	-	I	HDACTB#	39	40	GND	PWR	-	-	
	-	-	PWR	VCC	41	42	VCC	PWR	-	-	
	-	-	PWR	GND	43	44	NC	-	-	-	

4.5.3 CF Connector (CF)

This connector is mounted on the backside of the 786LCD-M/mITX. If a Compact Flash Disk is used, then no IDE drive can be connected to the IDE_S2 connector. The socket support DMA/UDMA modules.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	TBD	IO	DB3	2	1	GND	PWR	-	-	1
	-	TBD	IO	DB5	4	3	DB4	IO	TBD	-	
	/10K	TBD	IO	DB7	6	5	DB6	IO	TBD	-	
	-	-	PWR	GND	8	7	HDCSB0#	O	TBD	-	
	-	-	PWR	GND	10	9	GND	PWR	-	-	
	-	-	PWR	GND	12	11	GND	PWR	-	-	
	-	-	PWR	GND	14	13	5V	PWR	-	-	
	-	-	PWR	GND	16	15	GND	PWR	-	-	
	-	-	O	DAB2	18	17	GND	PWR	-	-	
	-	-	O	DAB0	20	19	DAB1	O	-	-	
	-	TBD	IO	D1	22	21	DB0	IO	TBD	-	
	-	-	-	NC	24	23	DB2	IO	TBD	-	
	-	-	-	NC	26	25	NC	-	-	-	
	-	TBD	IO	DB12	28	27	DB11	IO	TBD	-	
	-	TBD	IO	DB14	30	29	DB13	IO	TBD	-	
	-	TBD	O	HDCSB#	32	31	DB15	IO	TBD	-	
	-	TBD	O	IORB#	34	33	NC				
	-	-	PWR	5V	36	35	IOWB#	O	TBD	-	
	-	-	PWR	5V	38	37	IRQB	I	-	/10K	
				NC	40	39	GND	PWR	-	-	
	1K	-	I	IORDYB#	42	41	RESETB#			-	
	-	-	O	DDACKB#	44	43	DDRQB	I	-	/5K6	
	-	-	-	NC	46	45	NC	-	-	-	
	-	TBD	IO	DB9	48	47	DB8	IO	TBD	-	
1	-	-	PWR	GND	50	49	DB10	IO	TBD	-	2

Note 1: Pin is longer than average length of the other pins.
Note 2: Pin is shorter than average length of the other pins.

4.6 Serial ATA harddisk interface

Two serial ATA harddisk controllers are available on the board – a primary controller (SATA0) and a secondary controller (SATAB).

4.6.1 SATA Hard Disk Connector (SATA0, SATA1)

SATA0:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA0 TX+				
3	SATA0 TX-				
4	GND	PWR	-	-	
5	SATA0 RX-				
6	SATA0 RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA0 RX+ SATA0 RX-	Host transmitter differential signal pair
SATA0 TX+ SATA0 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

SATA1:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA1 TX+				
3	SATA1 TX-				
4	GND	PWR	-	-	
5	SATA1 RX-				
6	SATA1 RX+				
7	GND	PWR	-	-	

The signals used for the secondary Serial ATA harddisk interface are the following:

Signal	Description
SATA1 RX+ SATA1 RX-	Host transmitter differential signal pair
SATA1 TX+ SATA1 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

4.7 Firewire / IEEE1394 connector

The 786LCD/mITX supports two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s, and 400M bits/s.

4.7.1 IEEE1394 Connector (IEEE1394_0 and IEEE1394_1)

The pinout of the Firewire / IEEE1394 connector IEEE1394_0 and IEEE1394_1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				TPA0+/1+	1	2	TPA0-/1-				
				GND	3	4	GND				
				TPB0+/1+	5	6	TPB0-/1-				
1				+12V	7	8	+12V				1
				KEY	9	10	GND				

Note 1: The 12V supply for the IEEE1394 devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two IEEE1394 channels.

Signal	Description
TPA0+ TPA0– TPA1+ TPA1–	Differential signal pair A
TPB0+ TPB0– TPB1+ TPB1–	Differential signal pair B
+12V	+12V supply

4.8 Printer Port Connector (PRINTER).

The printer port connector is provided in a standard DB25 pinout.
The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1						
						14	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	2						
						15	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	3						
						16	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	4						
						17	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	5						
						18	GND	PWR	-	-	
	2K2	24/24	IO	PD4	6						
						19	GND	PWR	-	-	
	2K2	24/24	IO	PD5	7						
						20	GND	PWR	-	-	
	2K2	24/24	IO	PD6	8						
						21	GND	PWR	-	-	
	2K2	24/24	IO	PD7	9						
						22	GND	PWR	-	-	
	2K2	-	I	ACK#	10						
						23	GND	PWR	-	-	
	2K2	-	I	BUSY	11						
						24	GND	PWR	-	-	
	2K2	-	I	PE	12						
						25	GND	PWR	-	-	
	2K2	-	I	SLCT	13						

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

4.9 Serial Ports

Four RS232C serial ports are available on the 786LCD/mITX.

The typical interpretation of the signals in the Serial Ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.9.1 Serial Port1 DB9 Connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RI	I	-	/5K	
	-		O	DTR	4						
						8	CTS	I	-	/5K	
	-		O	TxD	3						
						7	RTS	O		-	
	/5K	-	I	RxD	2						
						6	DSR	I	-	/5K	
	/5K	-	I	DCD	1						

4.9.2 Serial Port2, Port3 & Port4 Pin Header Connectors.

The pinout of Port2, Port3 and Port4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: 5V supply is shared with supply pins in Port2/Port3/Port4 headers. The common fuse is 1.1A.

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Port1.

4.10 Ethernet connectors.

The 786LCD/mITX boards supports 3 channels of 10/100Mb Ethernet.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB LAN networks.

4.10.1 Ethernet connector 1 (ETHER1)

Ethernet connector 1 is mounted together with USB Ports 0 and 3.

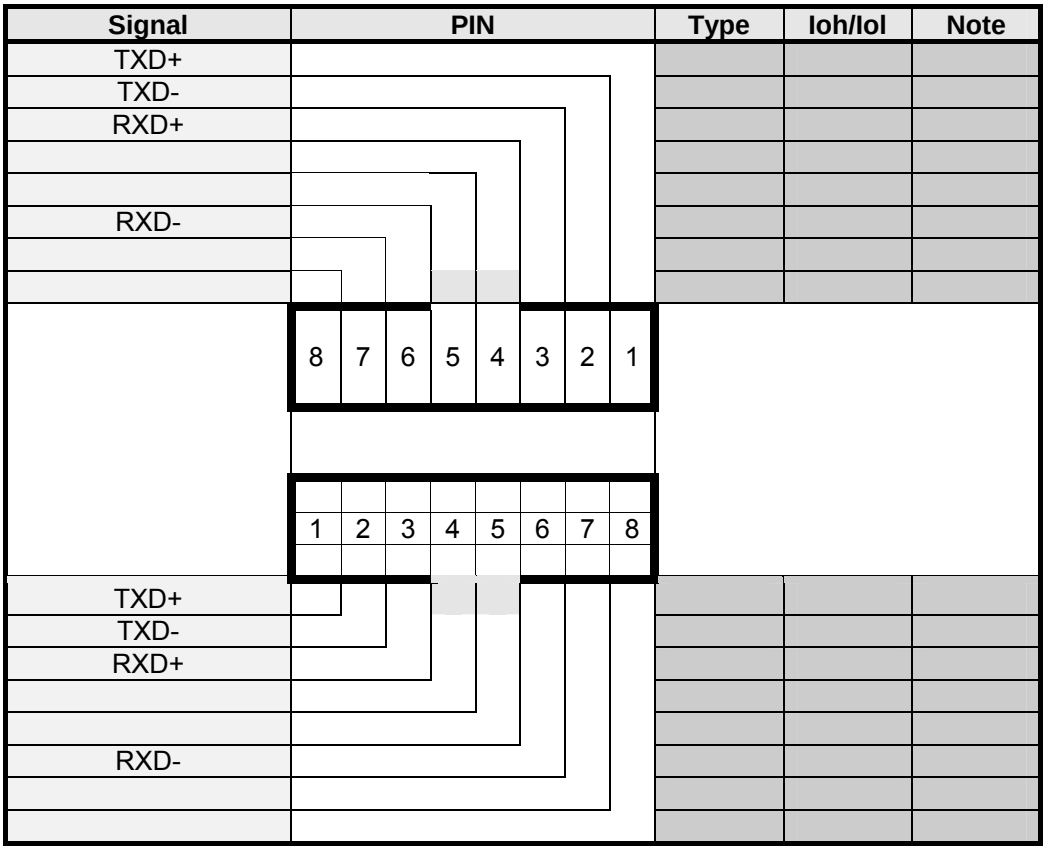
The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
TXD+				
TXD-				
RXD+				
RXD-				
	8 7 6 5 4 3 2 1			

4.10.2 Ethernet connector 2/3 (ETHER2/3)

The two Ethernet channels in ETHER2/3 are supported by two discrete Ethernet controllers (RTL8100C) connected to the onboard PCI bus.

The pinout of the RJ45's connector are as follows:



Note: The connector has two LEDs which indicates connection and traffic status. The left LED is status for the ETHER3 (buttom port) and the right LED is for ETHER2. More than one type of connector is approved for this application. Please notice that it is possible that the shape of the LED might vary depending on actual type of connector.

4.11 USB Connector (USB)

The ICH4 contains an Enhanced Host Controller Interface (EHCI) compliant host controller that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The ICH4 also contains three Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling with a total of 6 ports.

All six USB ports supports USB2.0 and USB1.1 and all ports supports Over-current detection.

USB Port 0 and 3 are supplied on the combined ETHER1, USB0, USB3 connector. USB Ports 1 and 4 are supplied on the FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out. USB Ports 2 and 5 are supplied on the USB25 connector.

USB Port 0, 1, 2 and 3 supports USB Legacy mode.

4.11.1 USB Connector 0/3 (USB0/3)

USB Ports 0 and 3 are mounted together with ETHER1 ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
			IO	USB3-		USB3+	IO			
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
			IO	USB0-		USB0+	IO			

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB v.1.1 standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB3+ USB3-	Differential pair works as Data/Address/Command Bus. Legacy USB is supported by both USB0 and USB3.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.11.2 USB Connector 2/5 (USB25)

The pinout of the USB connector USB25 (no Shroud) is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-	-	
			IO	USB2-	3	4	USB5-	IO			
			IO	USB2+	5	6	USB5+	IO			
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-		KEY		10	NC		-	-	

Signal	Description
USB2+ USB2- USB5+ USB5-	Differential pair works as Data/Address/Command Bus. Legacy USB is supported by USB2.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.12 Audio Connector

4.12.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	Line in – Left	IA	1
RING	Line in – Right	IA	1
SLEEVE	GND	PWR	
TIP	Line out – Left	OA	
RING	Line out – Right	OA	
SLEEVE	GND	PWR	
TIP	MIC 1	IA	1
RING	MIC 2	IA	1
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

4.12.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

4.12.3 AUDIO Header (AUDIO HEADER)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				SPKR_OUT_L	5	6	SPKR_OUT_R				
				AAGND	7	8	AAGND				
				SURR-OUT-L	9	10	SURR-OUT-R				
				NC	11	12	NC				
				AAGND	13	14	AAGND				
				F-FRONT-MIC1	15	16	F-FRONT-MIC2				
				AAGND	17	18	AAGND				
				F-AUX-IN-L	19	20	F-AUX-IN-R				
				F-MONO-OUT	21	22	AAGND				
	-	-	PWR	GND	23	24	F-SPDIF-IN				
				F-SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description
LFE-OUT	Low Frequency Effect Out channel (un-amplified)
CEN-OUT	Center Out channel (un-amplified)
SPKR_OUT_L SPKR_OUT_R	Speaker Out Left and Right Channel. Both signal are amplified to 3W.
SURR-OUT-L SURR-OUT-R	Surround Out Left and Right channel
NC	Not connected
F-FRONT-MIC1 F-FRONT-MIC2	Dedicated MIC Input 1, 2 for Frontpanel MIC
F-AUX-IN-L F-AUX-IN-R	AUX Left and Right Channel input
F-MONO-OUT	Speaker Phone Output
F-SPDIF-IN	S/PDIF Input, for coax cable
F-SPDIF-OUT	S/PDIF Output, for coax cable
AAGND	Audio Analogue ground

4.13 Fan connectors , SYSTEM FAN and CPU FAN.

The **SYSTEM FAN** can be used to power, control and monitor a fan for chassis ventilation etc.

The **CPU FAN** is used for connection of the active cooler for the CPU.

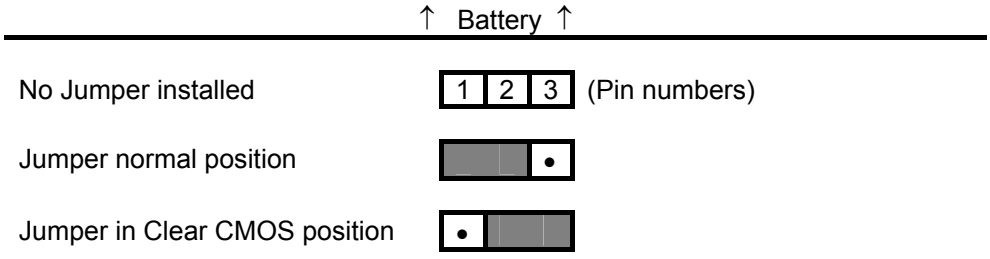
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE	PWR	-	4K7	
2	12V	PWR	-	-	
3	GND	PWR	-	-	

Signal description:

Signal	Description
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 800 mA can be supplied from this pin.
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.

4.14 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.



To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

4.15 LPC IFC connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	LPCCLK				
	-	-	PWR	GND	3	4	LPC AD0				
				LPC FRAME#	5	6	LPC AD1				
				INT SERIQ	7	8	LPC AD2				
				LPC DRQ#1	9	10	LPC AD3				

4.16 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	USB14_5V	1	2	USB14_5V	PWR	-	-	
				USB1-	3	4	USB4-				
				USB1+	5	6	USB4+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	Key		10	NC	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				3V3	19	20	NC	-	-	-	
				AGND	21	22	AGND				
				SPKR_OUT_L	23	24	SPKR_OUT_R				

Signal	Description
USB14_5V	+5V supply for the USB devices on USB Port 1 and 4 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB4+ USB4-	Universal Serial Bus Port 4 Differentials: Bus Data/Address/Command Bus. USB4 support Legacy.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX PSU and boot the board.
RSTIN#	Reset Input. Pull low to reset the board.
SPKR_OUT_L	Speaker Out Left channel, amplified, 3W
SPKR_OUT_R	Speaker Out Right channel, amplified, 3W
SB3V3	3.3V standby voltage
AGND	Analogue Ground for Audio

4.17 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol [mA]	Type	Signal	PIN		Signal	Type	Ioh/Iol [mA]	Pull U/D	Note
2	100K/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I			
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	+3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
3	2K7/	12/6	IO	GPIO0	11	12	GPIO1	IO	12/6	2K7/	3
3	2K7/	12/6	IO	GPIO2	13	14	GPIO3	IO	12/6	2K7/	3
4	2K7/	12/6	IO	GPIO4	15	16	GPIO5	IO	12/6	2K7/	4
4	2K7/	12/6	IO	GPIO6	17	18	GPIO7	IO	12/6	2K7/	4
	-	-	PWR	GND	19	20	FAN3OUT	AO			
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to 3V3 supply. Note 2: Pull-up to RTC-Voltage. Note 3: Pull-up to SB5V (standby +5V available on pin 5) and via 33R. Note 4: Pull-up to 5V supply.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
+3V3	
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND, for instance pin 10. The on board battery circuit makes sure that the external battery will not be recharged. The external battery can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC.
+5V	
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for Win98, WinXP, WinNT, and Win2000.
FAN3OUT	FAN 3 speed control OUTput (1), PWM (high impedanse) output signal to implement voltage in the range 0-4.7V in steps of 0.3V. This signal is shared with the BKLTCTL signal (available in LVDS Connector). This analogue voltage output controls the Fan3 speed. Windows API is available to operate the FAN3OUT (BKLTCTL) signal.
FAN3IN	FAN3 Input. 0V to +5V amplitude Fan 3 tachometer input.
+12V	
TEMP3IN	Temperature sensor 3 input. (F.eks Transistor 2N3904).
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

4.17.1 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE				**COMPONENT SIDE**			
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.17.2 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continued)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.17.3 786LCD PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
786LCD/mITX	1	AD16	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E.

5. Onboard Connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
SYSTEM FAN	Molex	22-23-2031	AMP	1375820-3
CPU FAN				
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA0	Molex	67491-0020	Molex	67489-8005
SATA1			Kontron	KT 821035 (cable kit)
ATXPWR	FoxConn	HM2510E	Molex	39-01-2205
COM2	Foxconn	HL20051	Molex	90635-1103
COM3			Kontron	KT 821016 (cable kit)
COM4			Kontron	KT 821017 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
			Kontron	KT 821044 (cable kit)
FRONTPNL	Foxconn	HL20121	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)
IDE_P	Foxconn	HL20201-UD2	Kontron	KT 821018 (cable kit)
IDE_S			Kontron	KT 821013 (cable kit)
IEEE1394_0	Foxconn	HC11051-P9	Kontron	KT 821040 (cable kit)
IEEE1394_1				
USB25	Foxconn	HC11051-P9	Kontron	KT 821401 (cable kit)
IDE_S2	Foxconn	HS5522V	AMP	2-111623-5
			Kontron	KT 821010 (cable kit)
			Kontron	KT 821012 (cable kit)
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)

6. System Ressources

6.1 Memory map

The table below lists the system memory map.

Address range (hex)		Size	Description
00000000-	0007FFFF	512 Kbytes	Conventional memory
00080000-	0009FBFF	127 Kbyte	Extended conventional memory
0009FC00-	0009FFFF	1 Kbyte	Extended BIOS data
000A0000-	000AFFFF	64 Kbytes	815 VGA Controller, Video memory and BIOS
000B0000-	000BFFFF	64 Kbytes	815 VGA Controller, Video memory and BIOS
000C0000-	000CBFFF	48 Kbytes	815 VGA Controller, Video memory and BIOS
000CC000-	000CDFFF	8 Kbytes	Realtek 8100 Ethernet boot.
F8000000-	FBFFFFFF	0x4000000	815 VGA Controller
FF8F8000-	FF8FBFFF	0x4000	TI Firewire - IEEE 1394
FF8FE800-	FF8FE8FF	0x100	Realtek 8100 Ethernet Controller
FF8FEC00-	FF8FECFF	0x100	Realtek 8100 Ethernet Controller
FF8FF000-	FF8FF7FF	0x800	TI Firewire - IEEE 1394
FF8FF800-	FF8FF8FF	0x100	Realtek 8100 Ethernet Controller
FF8FFC00-	FF8FFDFF	0x200	SATA/RAID controller
FFA7F400-	FFA7F7FF	0x400	USB Controller
FFA7F800-	FFA7F8FF	0x100	Realtek AC97 Audio
FFA7FC00-	FFA7FDFF	0x200	Realtek AC97 Audio
FFA80000-	FFAFFFFF	0x80000	815 VGA Controller
FFB7FC00-	FFB7FFFF	0x400	Ultra SATA Controller
FFB80000-	FFBFFFFF	0x80000	Intel 82802 Firmware Hub Device
FFF80000-	FFFFFFFF	0x80000	Intel 82802 Firmware Hub Device

6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	8086h	1130h	AD11	MCH	Host bridge
0	2	0	8086h	1132h	AD13	MCH	VGA controller
0	29	0	8086h	24C2h	AD40	6300ESB	USB
0	29	1	8086h	24C4h		6300ESB	USB
0	29	2	8086h	24C7h		6300ESB	USB
0	29	7	8086h	24CDh		6300ESB	USB
0	30	0	8086h	244Eh	AD41	6300ESB	Pci to Pci bridge
0	31	0	8086h	24C0h	AD42	6300ESB	ISA Bridge
0	31	1	8086h	24CBh		6300ESB	IDE Controller
0	31	3	8086h	24C3h		6300ESB	SMBus
0	31	5	8086h	24C5h		6300ESB	Audio
1	0	0	-	-	AD16	-	PCI slot #1
1	1	0	10ECh	8139h	AD17	RTL8100	Ethernet
1	2	0	10ECh	8139h	AD18	RTL8100	Ethernet
1	3	0	10ECh	8139h	AD19	RTL8100	Ethernet
1	4	0	104Ch	8023h	AD20	TI43AB22	IEEE 1394(Firewire)
1	5	0	1095h	3512h	AD21	SIL3512	SATA

Note: The PCI slot supports PCI BUS Mastering.

6.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Serial Port C	May be used by onboard Serial Port D	May be used by onboard SATA controller	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used for onboard Sound System	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard Ethernet controller 3	May be used by onboard 1394 (Firewire)	May be used by onboard SATA Controller	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQD depending on selections in the BIOS	Notes
NMI	•																										
IRQ0		•																									
IRQ1			•																								
IRQ2				•																							
IRQ3					•	•	•	•																		•	1, 2
IRQ4					•	•	•	•																		•	1, 2
IRQ5										•								•		•						•	1, 2
IRQ6					•	•	•	•			•															•	1, 2
IRQ7										•																•	1, 2
IRQ8												•															
IRQ9																	•	•	•			•			•	•	1, 2
IRQ10					•	•	•	•										•					•			•	1, 2
IRQ11					•	•	•	•										•			•			•		•	1, 2
IRQ12													•													•	1
IRQ13														•													
IRQ14															•											•	1
IRQ15																•										•	1
IRQ16																		•									3
IRQ17												•							•								3
IRQ18									•											•							3
IRQ19																		•			•						3
IRQ20																											3
IRQ21																											3
IRQ22																						•					3
IRQ23																		•					•				3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQH can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ23 are APIC interrupts

6.4 I/O Map

Address (hex)		Size	Description
0020-	0021	2	Programmable interrupt controller
0040-	0043	4	System Timer
0060-	0060	1	Standard keyboard
0061-	0061	1	System speaker
0070-	0071	2	System CMOS/Real time clock
0170-	01F7	8	Secondary Parallel ATA IDE Channel
01F0-	01F7	8	Primary Parallel ATA IDE Channel
02E8-	02EF	8	Comport 4
02F8-	02FF	8	Comport 2
0378-	037F	8	Printer Port
03B0-	03BB	0xC	815 VGA Controller
03C0-	03DF	0x20	815 VGA Controller
03E8-	03EF	8	Comport 3
03F8-	03FF	8	Comport 1
0CF8-	0CFF	8	PCI Bus
C400-	C4FF	0x100	Realtek 8100 Ethernet Controller
C800-	C8FF	0x100	Realtek 8100 Ethernet Controller
D000-	D0FF	0x100	Realtek 8100 Ethernet Controller
D400-	D40F	0x10	SATA/Raid Controller
D480-	D483	4	SATA/Raid Controller
D800-	D807	8	SATA/Raid Controller
D880-	D883	4	SATA/Raid Controller
DC00-	DC07	8	SATA/Raid Controller
E000-	E01F	0x20	Standard Universal PCI to USB Host Controller
E080-	E09F	0x20	Standard Universal PCI to USB Host Controller
E400	E41F	0x20	Standard Universal PCI to USB Host Controller
E480-	E49F	0x20	PCI System Management Bus
E800-	E8FF	0x100	Realtek AC97 Audio
EC00-	EC3F	0x40	Realtek AC97 Audio
FFA0-	FFAF	0x10	Ultra ATA Controller

6.5 DMA Channel Usage

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

7. Overview of BIOS features

This Manual section details specific BIOS features for the 786LCD/mITX boards.
The 786LCD/mITX boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

7.1.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

The 786LCD/mITX Boards supports reading certain MIF specific details by the Windows API. Refer to the API section in this manual for details.

7.1.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

8. BIOS Configuration / Setup

8.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the 786LCD/mITX board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

```
                         BIOS SETUP UTILITY
   Main     Advanced     PCIPnP     Boot     Security     Chipset     Power     Exit
```

The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

8.2 Main Menu

```
                         BIOS SETUP UTILITY
   Main     Advanced     PCIPnP     Boot     Security     Chipset     Power     Exit
 System Overview                                          Use [ENTER], [TAB] or
                                                          [SHIFT-TAB] to select
 AMIBIOS                                                  a field.
 Version    : 08.00.10
 Build Date: 05/25/07                                     Use [+] or [-] to
 ID         : 786LCD11                                    configure system Time.
 PCB ID     : 82
 Serial #   : 00375346
 PCB ID     : 63520001

 Processor
 Type       : Intel(R) Pentium (R) III CPU - S            <-   Select Screen
 Speed      : 733MHz                                      ||   Select Item
                                                          +-   Change Field
 System Memory                                            Tab  Select Field
 Size       : 255MB                                       F1   General Help
 Speed      : 133MHz                                      F10  Save and Exit
                                                          ESC  Exit
 System Time                    [15:18:15]
 System Date                    [Fri 05/30/2008]

          V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

Main Menu Selections

You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

8.3 Advanced Menu

```
                        BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  Advanced Settings                          | Configure CPU.
  Warning: Setting wrong values in below sections
           May cause system to malfunction.
> CPU Configuration
> IDE Configuration
> LAN Configuration
> SATA/RAID Configuration
> FW/IEEE 1394 Configuration
> SuperIO Configuration
> Voltage Monitor                           | <-    Select Screen
> Hardware Health Configuration             | ||    Select Item
> Remote Access Configuration               | Enter Go to Sub Screen
> USB Configuration                         | F1    General Help
> ACPI Configuration                        | F10   Save and Exit
                                            | ESC   Exit
                  V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

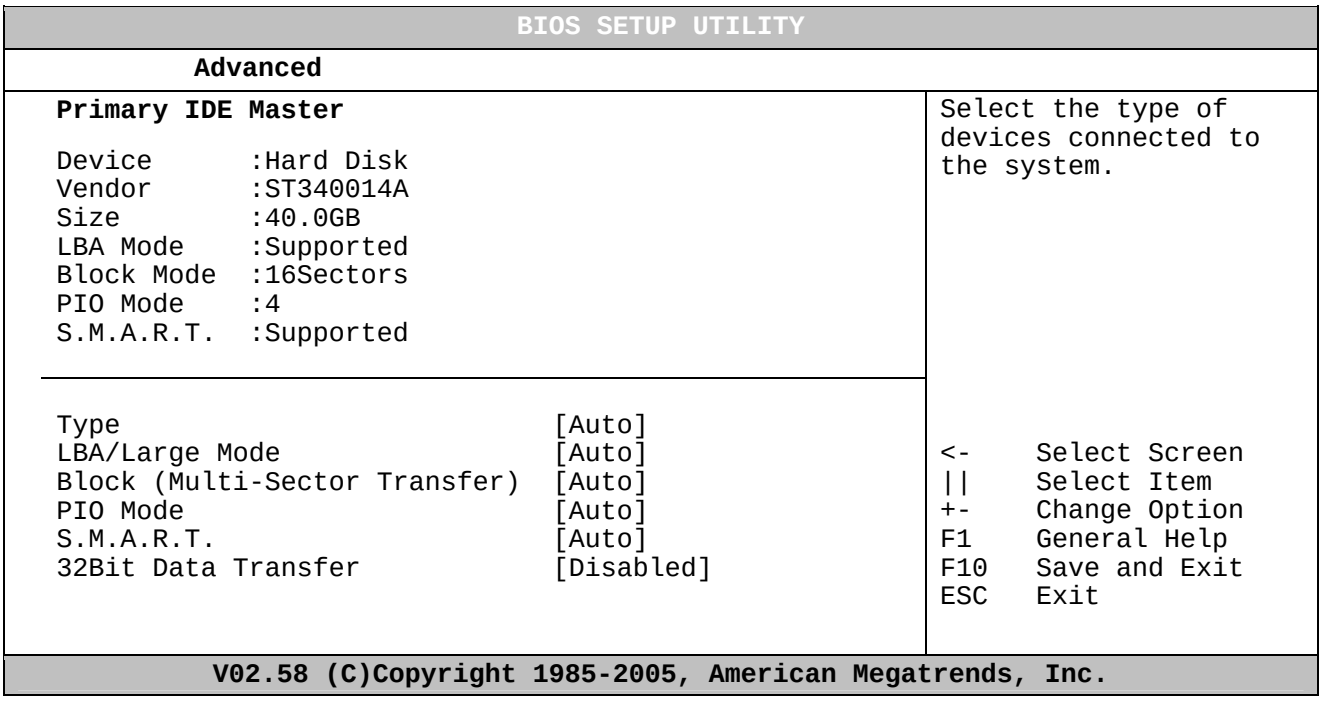
8.3.1 Advanced settings – CPU Configuration

```
                        BIOS SETUP UTILITY
                             Advanced
  Configure advanced CPU settings           |
  Manufacturer: Intel
  Brand String: Intel (R) Pentium (R) III CPU - S
  Frequency   : 733MHz
  Ratio Status: Locked                      | <-    Select Screen
                                            | ||    Select Item
                                            | +-    Change Option
                                            | F1    General Help
                                            | F10   Save and Exit
                                            | ESC   Exit
                  V02.58 (C)Copyright 1985-2005, American Megatrends, Inc..
```

8.3.2 Advanced settings – IDE Configuration

```
                        BIOS SETUP UTILITY
                              Advanced
   IDE Configuration                                  DISABLED: disables the
   OnBoard PCI IDE Controller     [Both]              integrated IDE
                                                      controller.
>  Primary IDE Master                : [Not Detected] PRIMARY: enables only
>  Primary IDE Slave                 : [Not Detected] the Primary IDE
>  Secondary IDE Master              : [Not Detected] controller.
>  Secondary IDE Slave               : [Not Detected] SECONDARY: enables
                                                      only the Secondary IDE
   Hard Disk Write Protect        [Disabled]          controller.
   IDE Detect Time Out (Sec)      [35]                BOTH: enables both IDE
   ATA(PI) 80Pin Cable Detection  [Host & Device]     controllers.
   P-ATA1 Cable Detection force   [Disabled]
   P-ATA2 Cable Detection force   [Disabled]
                                                      <-    Select Screen
                                                      ||    Select Item
                                                      +-    change option
                                                      F1    General Help
                                                      F10   Save and Exit
                                                      ESC   Exit
                  V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

Feature	Options	Description
OnBoard PCI IDE Controller	Disable Primary Secondary **Both**	Setup the configuration of the hard drive interfaces



Feature	Options	Description
Type	Not Installed **Auto** CDROM ARMD	Select the type of device installed
LBA/Large Mode	Disabled **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto** 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
S.M.A.R.T.	**Auto** Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	**Disabled** Enabled	Select if the Device should be using 32Bit data Transfer

Feature	Options	Description
Hard Disk Write Protect	**Disable** Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Select the time out value when the BIOS is detecting ATA/ATAPI Devices
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Select the mechanism for detecting 80Pin ATA Cable
P-ATA1 Cable Detection Force	**Disable** 40Pin 80Pin	Force the board to operate as if a 40Pin ATA cable or 80Pin ATA cable is installed on the Primary channel
P-ATA2 Cable Detection Force	**Disable** 40Pin 80Pin	Force the board to operate as if a 40Pin ATA cable or 80Pin ATA cable is installed on the Primary channel

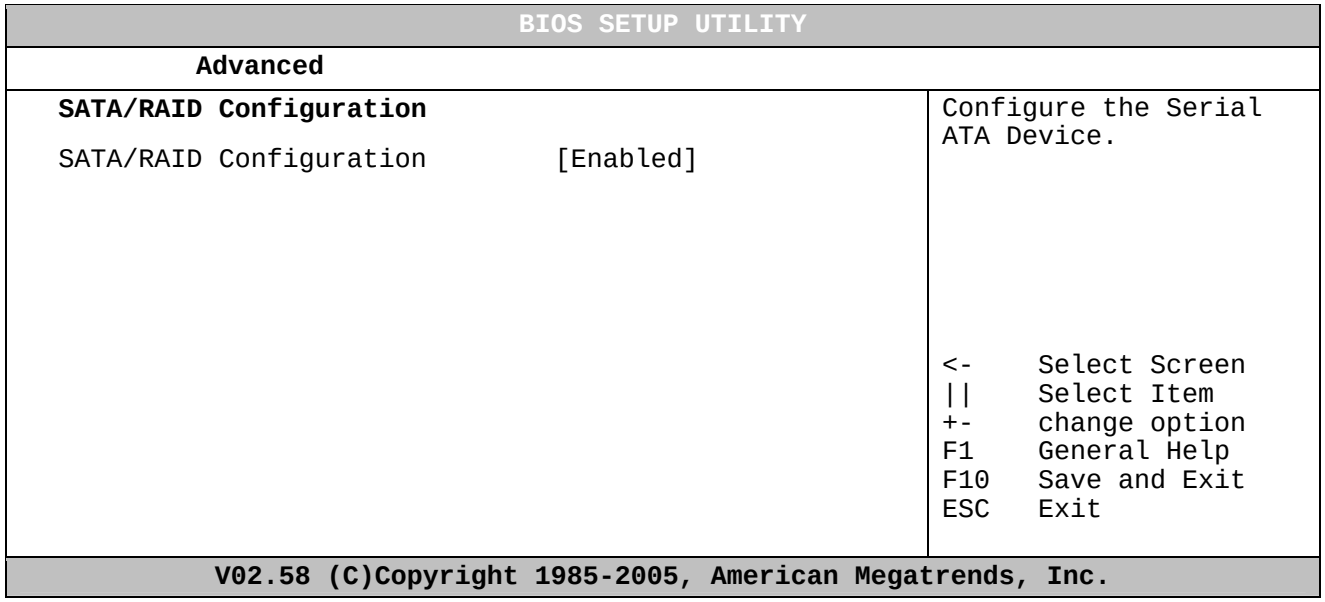
8.3.3 Advanced settings – LAN Configuration

```
                        BIOS SETUP UTILITY
                              Advanced
  LAN Configuration                                  Control of Ethernet
                                                     Devices and PXE boot
  ETH1 Configuration                [Enabled]
    MAC Address                     : 00E0F4140E26
  ETH2 Configuration (Upper)        [Enabled]
    MAC Address                     : 00E0F4140E27
  ETH3 Configuration (Lower)        [Enabled]
    MAC Address                     : 00E0F4140E28

                                                     <-    Select Screen
                                                     ||    Select Item
                                                     +-    change option
                                                     F1    General Help
                                                     F10   Save and Exit
                                                     ESC   Exit
          V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

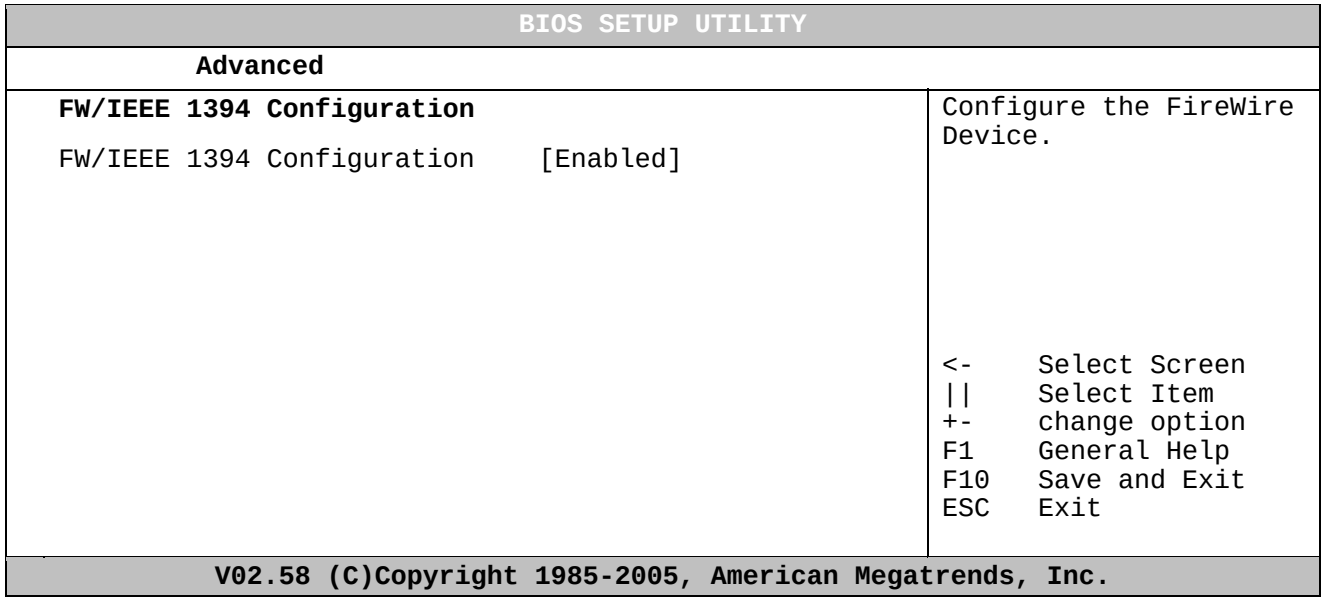
Feature	Options	Description
ETH1 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH2 Configuration (Upper)	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH3 Configuration (Lower)	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom

8.3.4 Advanced settings – SATA/RAID Configuration



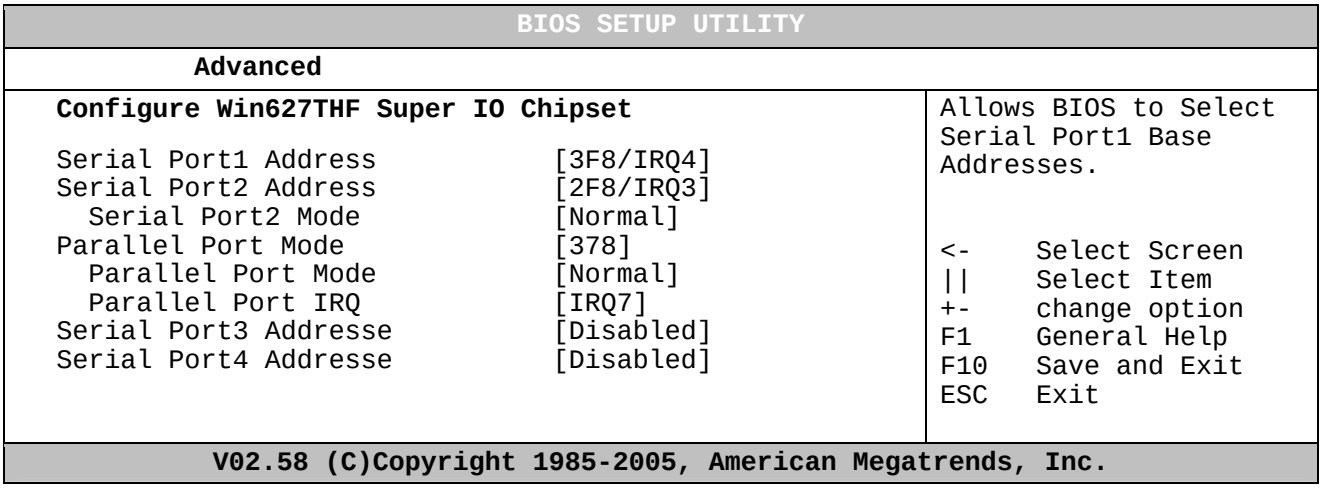
Feature	Options	Description
SATA/RAID Configuration	**Enabled** Disabled	Select SATA/RAID. (See chapter "How to Install SATA and RAID while installing Windows XP).

8.3.5 Advanced settings – FW/IEEE 1394 Configuration



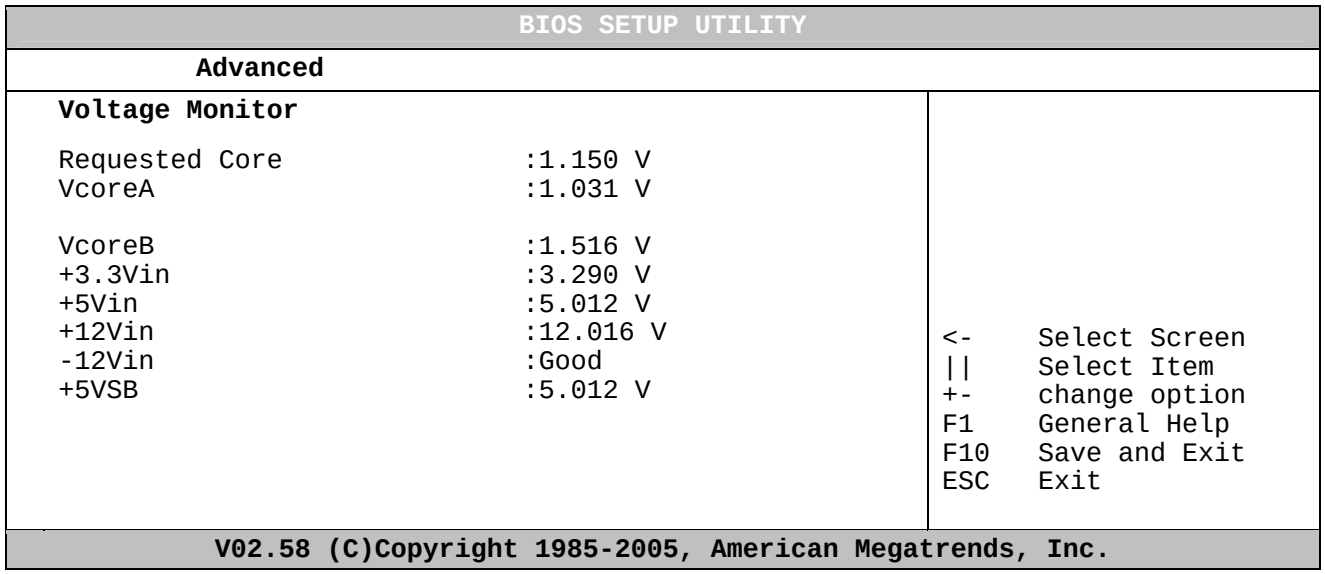
Feature	Options	Description
FW/IEEE 1394 Configuration	**Enabled** Disabled	Select FW/IEEE 1394

8.3.6 Advanced settings – SuperIO Configuration

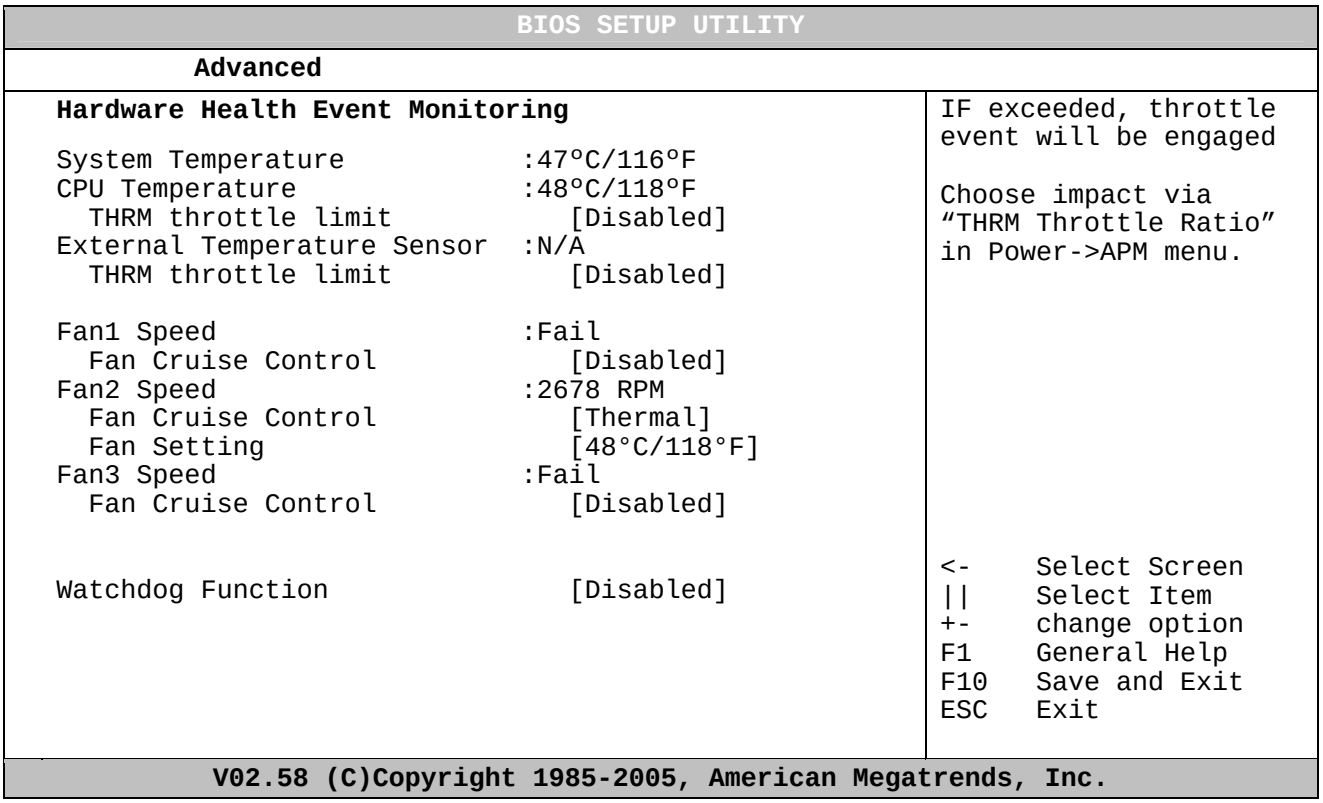


Feature	Options	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 3E8/IRQ4 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Address	Disabled **2F8/IRQ3** 2E8/IRQ3 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Mode	**Normal** IRDA ASK IR	Select Mode for Serial Port2
Parallel Port Address	Disabled **378** 278 3BC	Select the I/O address for the LPT.
Parallel Port Mode	**Normal** Bi-Directional EPP ECP	Select the mode that the parallel port will operate in
EPP Version	**1.9** 1.7	Setup with version of EPP you want to run on the parallel port
ECP Mode DMA Channel	DMA0 DMA1 **DMA3**	Select a DMA channel
Parallel Port IRQ	IRQ5 **IRQ7**	Select a IRQ
ICH SIO Serial Port1 Address	**Disabled** 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
ICH SIO Serial Port2 Address	**Disabled** 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).

8.3.7 Advanced settings – Voltage Monitor

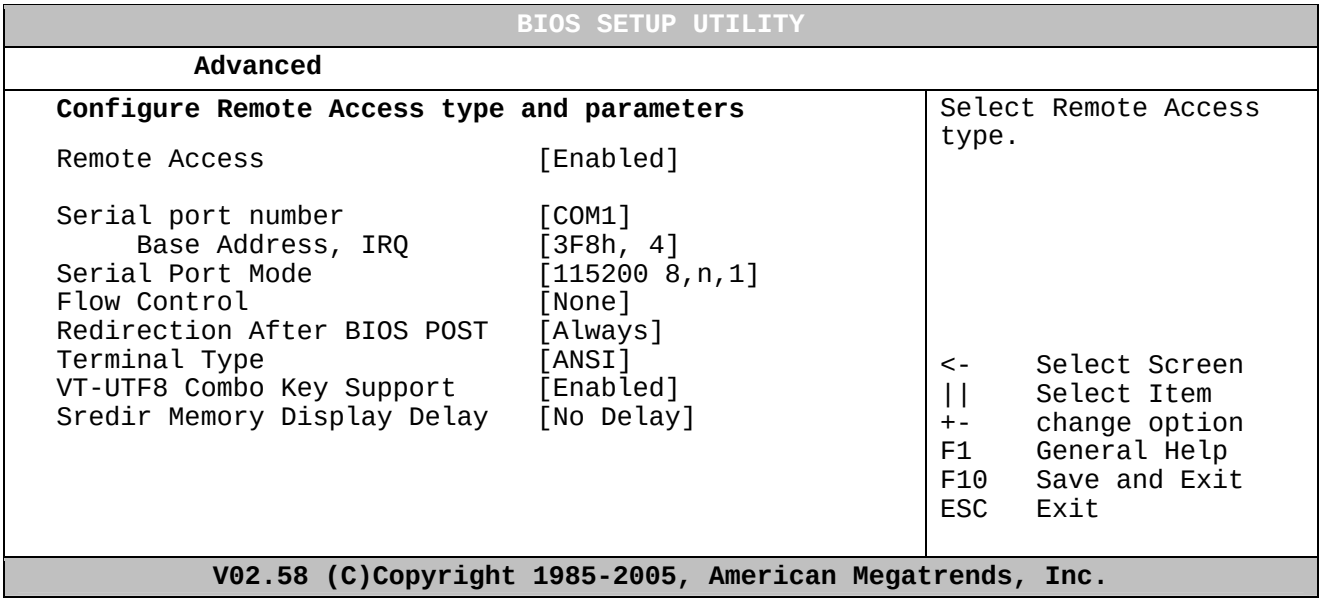


8.3.8 Advanced settings – Hardware Health Configuration



Feature	Options	Description
THRM throttle limit	**Disabled** 38°-80°C (100°-176°F)	IF exceeded, throttle event will be engaged. Choose impact via "THRM Throttle Ratio" in Power->APM menu.
Fan Cruise Control	**Disabled** Thermal Speed	Fan1 is System Fan. Fan2 is CPU Fan. Fan3 is Auxilary Fan (via Feature Connector). When set to Thermal, the Fan will be controlled by the corresponding temperature sensor (See Fan Settings below) When set to Speed, the Fan will be running at the Fixed speed set by Fan Settings below.
Fan Settings	1406-5625 RPM 30°-75°C (86°-167°F)	The fan can operate in Thermal mode or in a fixed fan speed mode
Watchdog Function	**Disabled** 32 seconds 76 seconds	Select either 32 or 76 seconds for the boot process until the Watch Dog service reloads the counter on address IO460h. The value for the counter shall be in the range 04h – 3Fh corresponding to 2.4 - 38 sec. in steps of 0.6 sec. The Watchdog can be disabled/enabled by writing to the address IO 469h Bit 3.

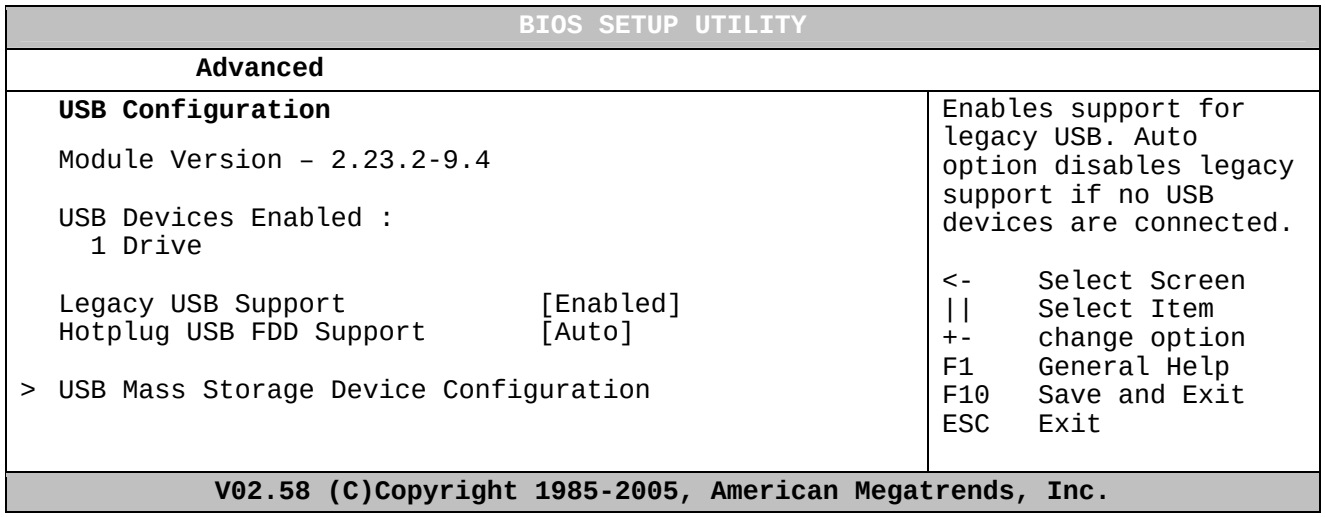
8.3.9 Advanced settings – Remote Access Configuration



```
                        BIOS SETUP UTILITY
                              Advanced
  Configure Remote Access type and parameters     | Select Remote Access
                                                  | type.
  Remote Access                 [Enabled]         |
                                                  |
  Serial port number            [COM1]            |
       Base Address, IRQ        [3F8h, 4]         |
  Serial Port Mode              [115200 8,n,1]    |
  Flow Control                  [None]            |
  Redirection After BIOS POST   [Always]          |
  Terminal Type                 [ANSI]            |
  VT-UTF8 Combo Key Support     [Enabled]         | <-    Select Screen
  Sredir Memory Display Delay   [No Delay]        | ||    Select Item
                                                  | +-    change option
                                                  | F1    General Help
                                                  | F10   Save and Exit
                                                  | ESC   Exit
                        V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

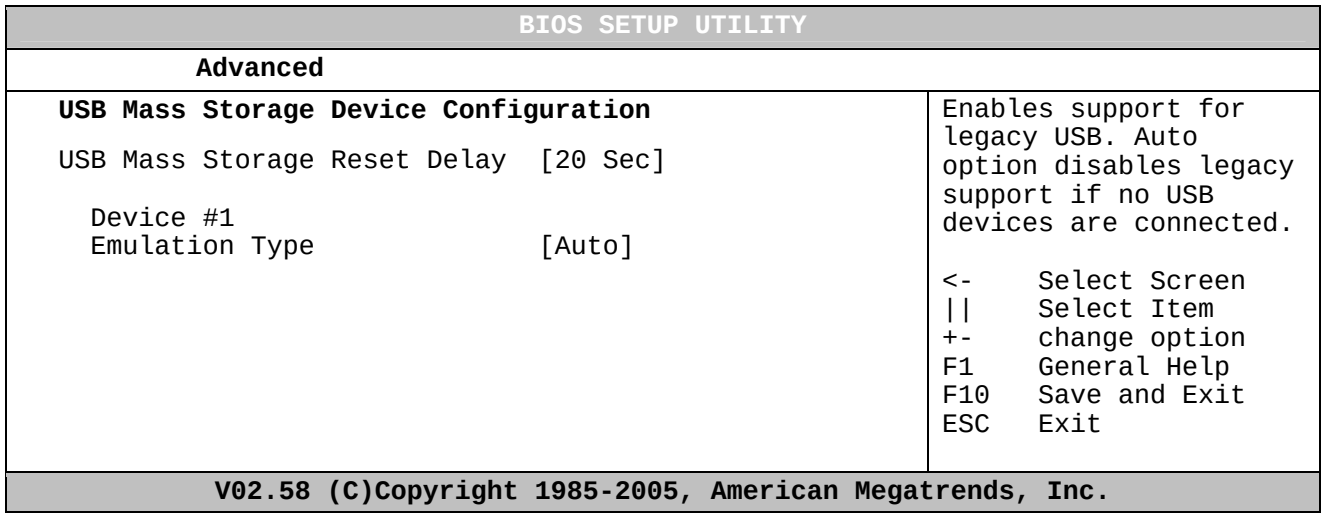
Feature	Options	Description
Remote Access	**Disabled** Enabled	Allows you to see the screen over the comport interface, in a terminal window
Serial port number	**COM1** COM2	Setup which comport that should be used for communication
Serial Port Mode	**115200 8 n 1** 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	**None** Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader **Always**	How long shall the BIOS send the picture over the serial port
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	Disabled **Enabled**	Setup VT-UTF8 Combo Key
Sredir Memory Display Delay	**No Delay** Delay 1 sec Delay 2 sec Delay 4 sec	Gives the delay in seconds to display memory information

8.3.10 Advanced settings – USB Configuration



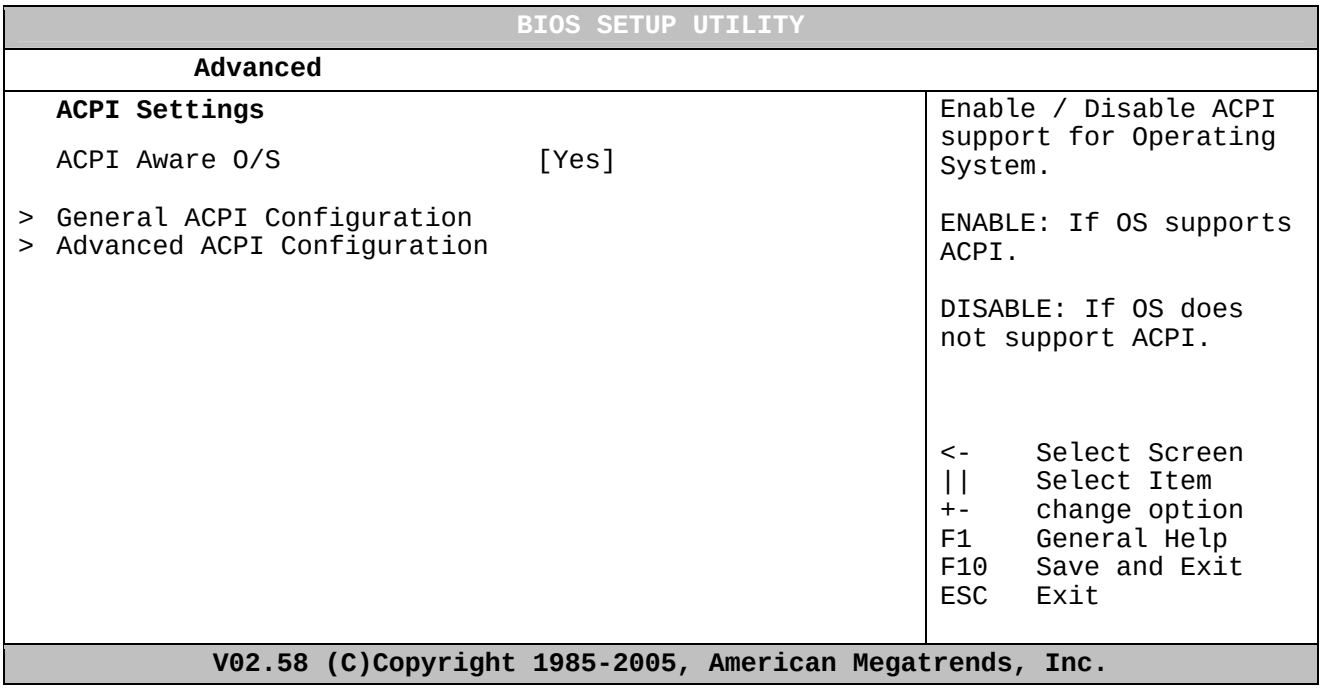
Feature	Options	Description
Legacy USB Support	Disabled **Enabled** Auto	Support for legacy USB Keyboard etc. connected to USB0, USB1, USB2 or USB3.
Hotplug USB FDD Support	Disabled Enabled **Auto**	A dummy FDD device is created that will be associated with the hotplugged FDD later. Auto option creates this dummy device only if there is no USB FDD present.

8.3.11 Advanced settings – USB Mass Storage Device Configuration



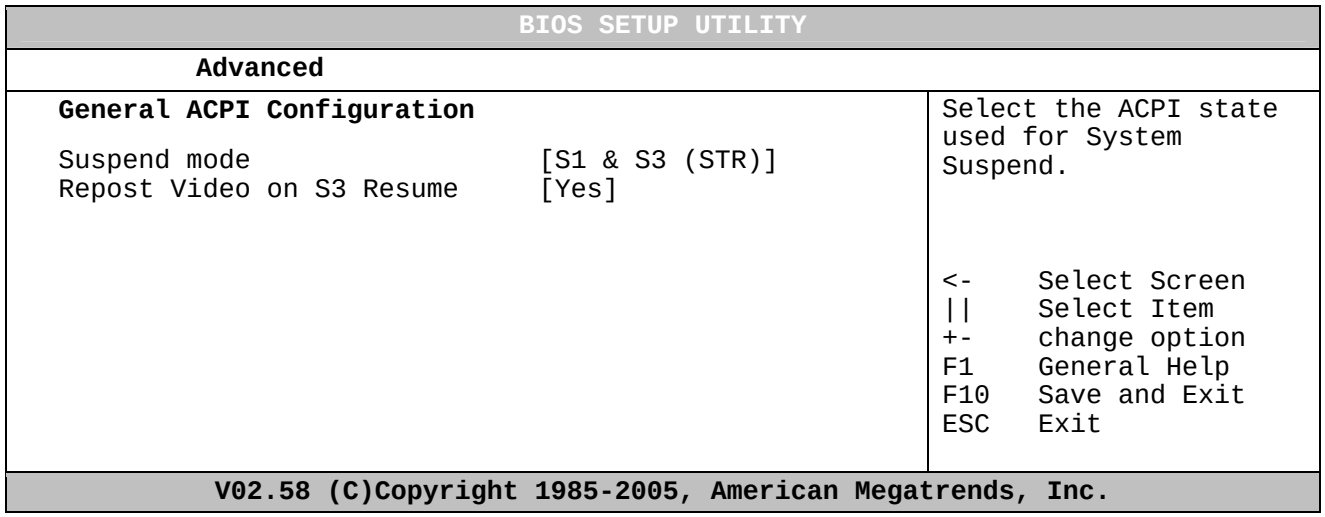
Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

8.3.12 Advanced settings – ACPI Settings



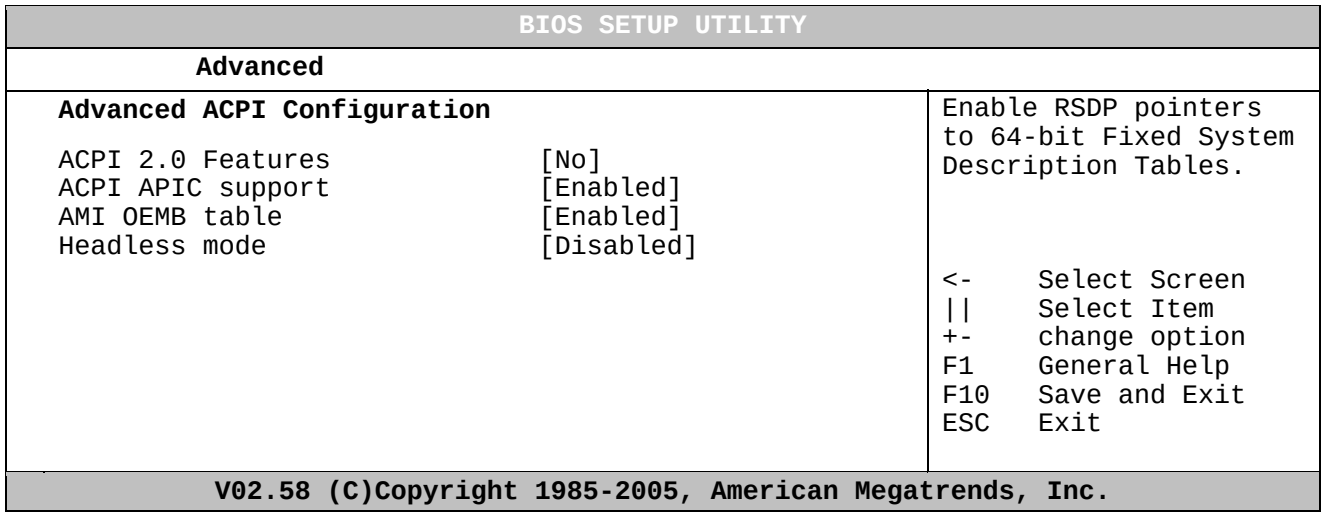
Feature	Options	Description
ACPI Aware O/S	**Yes** No	Select if O/S supports ACPI

8.3.13 Advanced settings – General ACPI Configuration



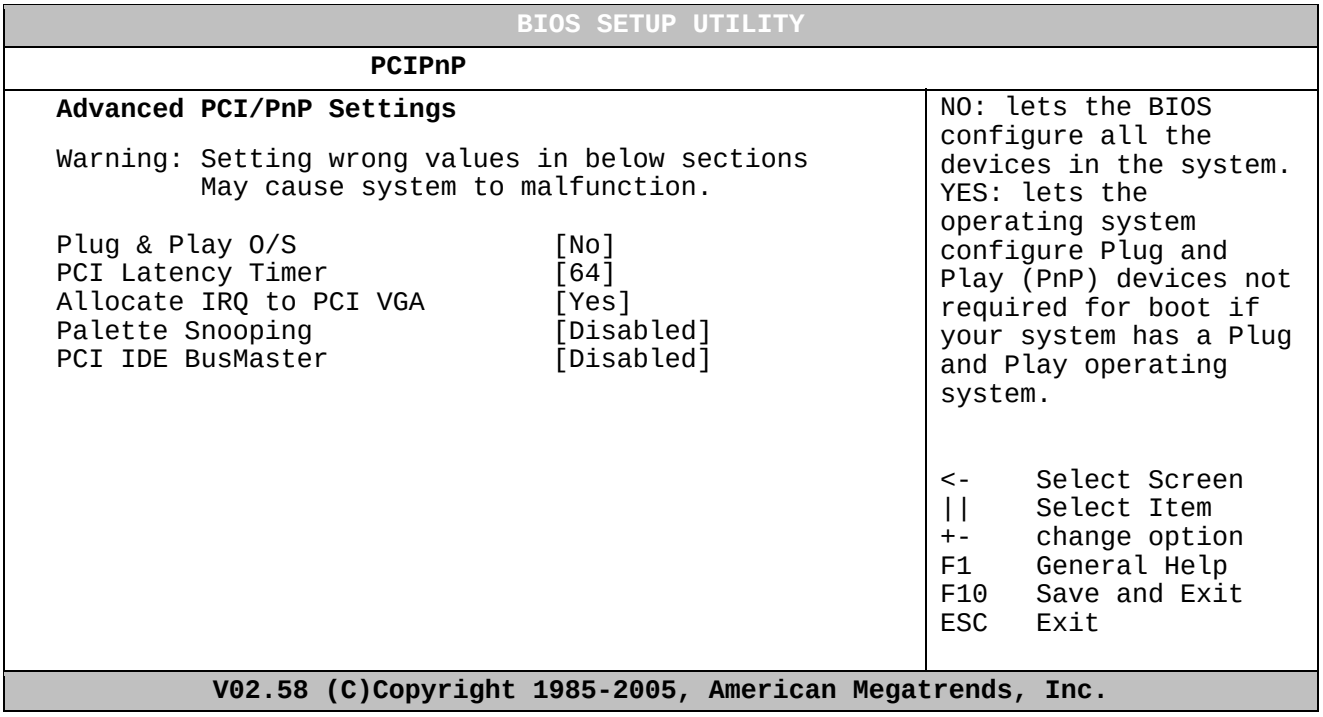
Feature	Options	Description
Suspend mode	S1 (POS) only **S1 & S3 (STR)**	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	No **Yes**	Determines whether to invoke VGA BIOS post on S3/STR resume

8.3.14 Advanced settings – Advanced ACPI Configuration



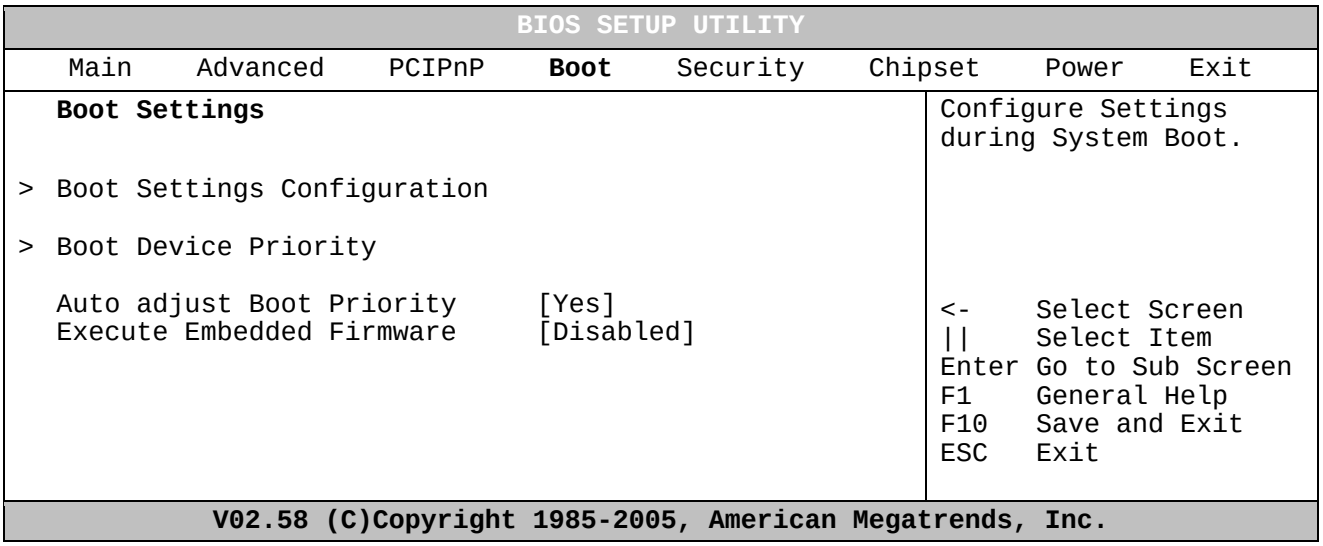
Feature	Options	Description
ACPI 2.0 Features	**No** Yes	Enable/ Disable ACPI 2.0 features
ACPI APIC support	**Enabled** Disabled	Setup if the APIC controller should be supported in the ACPI code
AMI OEMB table	**Enabled** Disabled	Enable/ Disable AMI OEMB table
Headless mode	Enabled **Disabled**	Enable/ Disable Headless mode

8.4 PCIPnP Menu



Feature	Options	Description
Plug & Play O/S	**No** Yes	Select if you have a PnP O/S
PCI Latency Timer	32 **64** 96 128 160 192 224 248	Value in units of PCI clocks for PCI device latency timer register
Allocate IRQ to PCI VGA	**Yes** No	Assigns IRQ to PCI VGA card
Palette Snooping	**Disabled** Enabled	ENABLED: informa the PCI devices that an ISA graphic device is installed in the system so the card will function correctly
PCI IDE BusMaster	Enabled **Disabled**	Setup PCI bus mastering for read/write to IDE drives

8.5 Boot Menu


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Power Exit
Boot Settings
> Boot Settings Configuration
> Boot Device Priority
Auto adjust Boot Priority [Yes]
Execute Embedded Firmware [Disabled]
Configure Settings during System Boot.
<- Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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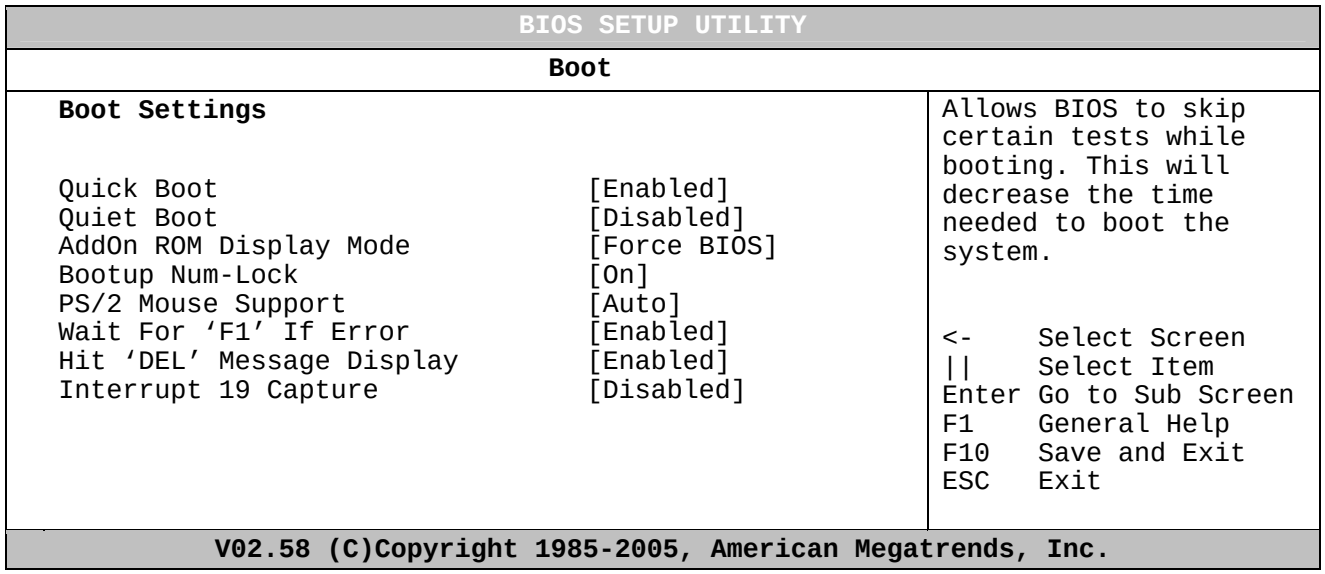
8.5.1 Boot – Boot Settings Configuration

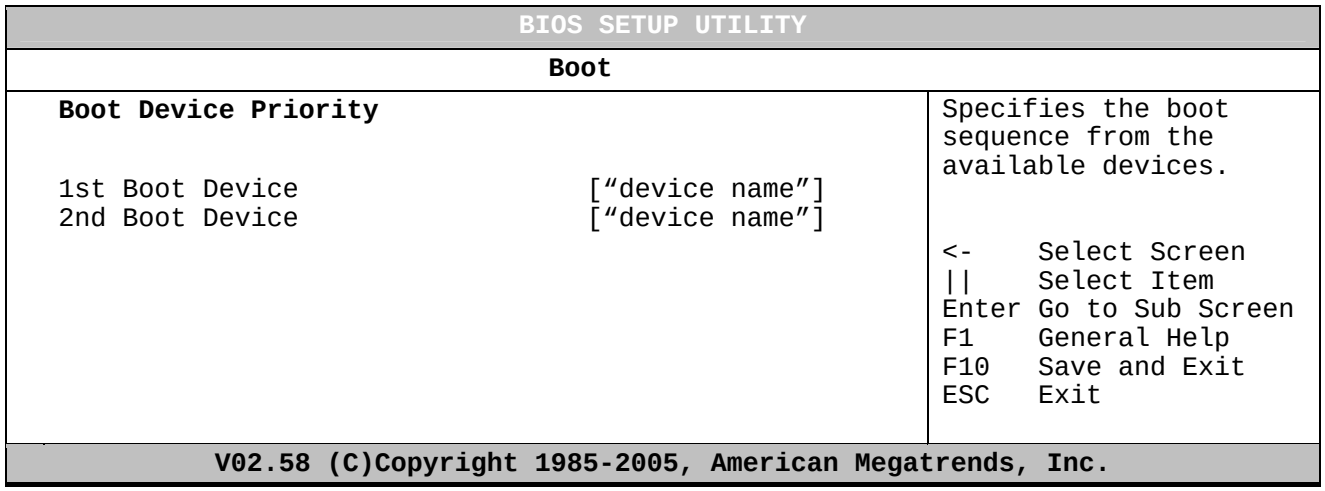


Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain test while booting
Quiet Boot	**Disabled** Enabled	Shows boot logo instead of POST screen
AddOn BIOS ROM Display Mode	**Force BIOS** Keep Current	
Bootup Num-Lock	Off **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse
Wait For 'F1' If Error (see note)	**Enabled** Disabled	Wait for F1 key to be pressed if error. If no keyboard present post will continue
Hit 'DEL' Message Display	Disabled **Enabled**	Display the message or not
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap interrupt 19

Note: List of errors:

<INS> Pressed
Timer Error
Interrupt Controller-1 error
Keyboard/Interface Error
Halt on Invalid Time/Date
NVRAM Bad
Primary Master Hard Disk Error
S.M.A.R.T HDD Error
Cache Memory Error
DMA Controller Error
Resource Conflict
Static Resource Conflict
PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table error

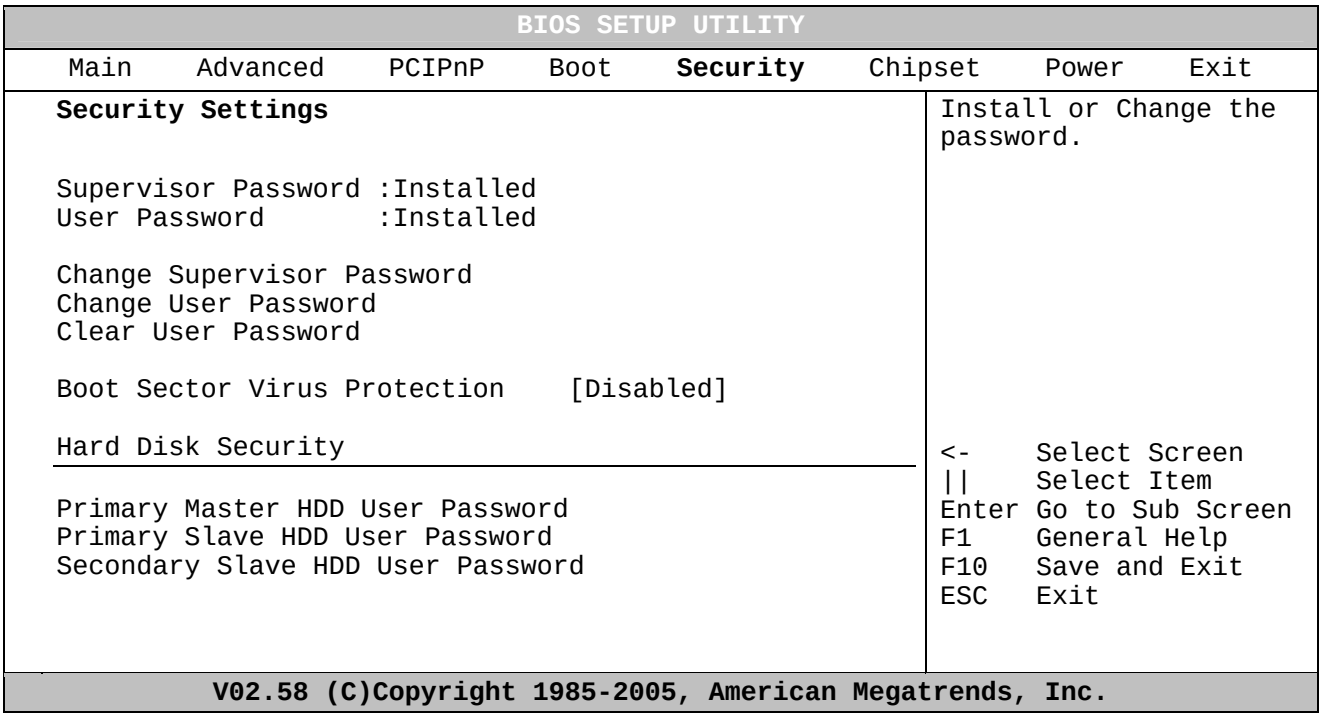
8.5.2 Boot – Boot Device Priority



Feature	Options	Description
1st Boot Device	“device names” Disabled	Name of the selected first boot device.
2nd Boot Device	“device names” Disabled	Name of the selected second boot device.

Feature	Options	Description
Auto adjust Boot Priority	**Yes** No	If Yes then eg. USB devices will be placed first in the boot Device Priority Menu when booting.
Execute Embedded Firmware	**Disabled** Enabled	Execute OEM software if embedded into BIOS. (Default MemTest-86)

8.6 Security Menu



Feature	Options	Description
Change Supervisor Password	Password	Change the Supervisor Password
Change User Password	Password	Change the User Password
Clear User Password	Ok Cancel	Clears the User Password
Boot Sector Virus Protection	Enabled **Disabled**	Will write protect the MBR when the BIOS is used to access the harddrive
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on

8.7 Chipset Menu

```
                        BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  Advanced Chipset Settings                          Intel ICH4 SouthBridge
                                                     chipset configuration
  Warning: Setting wrong values in below sections    options.
           may cause system to malfunction.

> Intel ICH4 SouthBridge Configuration

  System Memory Frequency          [Auto]
  Primary Video Device             [Auto]
  Display Cache Window Size        [ 64MB]
  Internal Graphic Scaling         [Auto]            <-    Select Screen
  Output Device Sync/Non-sync      [Non-synchronous] ||    Select Item
  AGP Graphic Aperture Size        [ 64MB]           Enter Go to Sub Screen
                                                     F1    General Help
  Backlight Signal Inversion       [Enabled]         F10   Save and Exit
  LCDVCC Voltage                   [3.3V]            ESC   Exit
  LVDS                             [Disabled]
  DVI                              [N/A]
                        V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

8.7.1 Advanced Chipset Settings – Configure advanced settings for SouthBridge

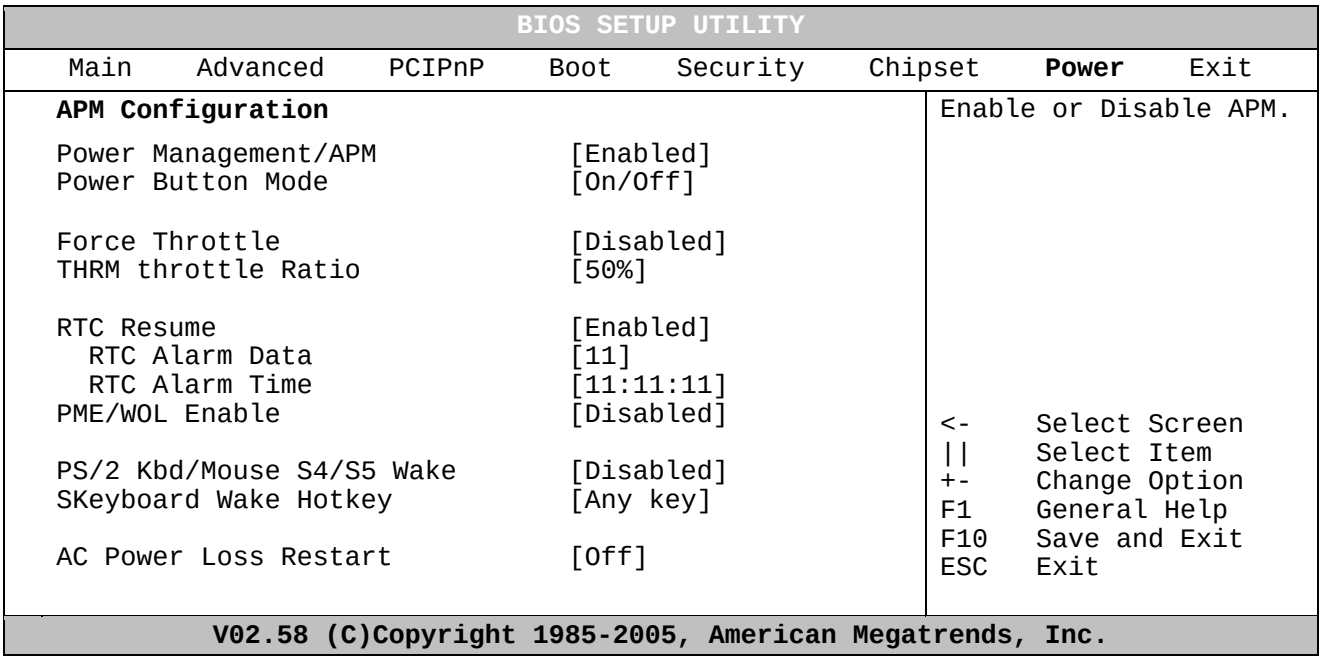
```
                        BIOS SETUP UTILITY
                                                     Chipset
  Configure advanced settings for SouthBrigde        Enable / Disable ICH4
                                                     IDE Controller
  ICH4 Dev31 Func1, IDE            [Enabled]         function.
  ICH4 Dev31 Func3, SMBUS          [Enabled]
  ICH4 Dev31 Func5, AC'97          [Enabled]
  OnBoard Amplifier                [Enabled]
  ICH4 Dev29 Func0, USB#1          [Enabled]
  ICH4 Dev29 Func1, USB#2          [Enabled]
  ICH4 Dev29 Func2, USB#3          [Enabled]
  ICH4 Dev29 Func7, ECHI           [Enabled]         <-    Select Screen
                                                     ||    Select Item
  Sound Blaster Decode             [Disabled]        Enter Go to Sub Screen
  Microsoft Sound Decode           [Disabled]        F1    General Help
  MIDI Decode                      [Disabled]        F10   Save and Exit
  Adlib Range 388h-38Bh            [Enabled]         ESC   Exit

  IOAPIC                           [Enabled]
  Extended IOAPIC                  [Enabled]
  CPU B.I.S.T                      [Disabled]
  ICH4 DMA Collection              [Enabled]
                        V02.58 (C)Copyright 1985-2005, American Megatrends, Inc.
```

Feature	Options	Description
ICH4 Dev31 Func1, IDE	Disabled, **Enabled**	Enable / Disable ICH4 IDE Controller function.
ICH4 Dev31 Func3, SMBUS	Disabled, **Enabled**	Enable / Disable ICH4 SMBUS Controller function.
ICH4 Dev31 Func5, AC'97	Disabled, **Enabled**	Enable / Disable ICH4 AC97 Controller function.
OnBoard Amplifier	Disabled, **Enabled**	Enable / Disable Audio Amplifier function.
ICH4 Dev29 Func0, USB#1	Disabled, **Enabled**	Enable / Disable ICH4 USB Controller#1 function.
ICH4 Dev29 Func1, USB#2	Disabled, **Enabled**	Enable / Disable ICH4 USB Controller#2 function.
ICH4 Dev29 Func2, USB#3	Disabled, **Enabled**	Enable / Disable ICH4 USB Controller#3 function.
ICH4 Dev29 Func7, ECHI	Disabled, **Enabled**	Enable / Disable ICH4 ECHI USB Controller function.
Sound Blaster Decode	**Disabled** 220h-233h 240h-253h 260h-273h 280h-293h	Enable / Disable Sound Blaster Decode.
Microsoft Sound Decode	**Disabled** 530h-537h 604h-60Bh E80h-E87h F40h-F47h	Choose which range to decode for the Microsoft Sound.
MIDI Decode	**Disabled** 330h-331h 300h-301h	Choose which range to decode for the MIDI port.
Adlib Range 388h-38Bh	Disabled, **Enabled**	Enable decoding of I/O locations 388h – 38Bh to the LPC interface.
IOAPIC	Disabled, **Enabled**	Enable / Disable ICH4 IOAPIC function
Extended IOAPIC	Disabled, **Enabled**	Enable / Disable the extended mode of ICH4 IOAPIC.
CPU B.I.S.T	**Disabled**, Enabled	Enable / Disable CPU Built In Self Test.
ICH4 DMA Collection	Disabled, **Enabled**	Enable / Disable DMA collection buffer.

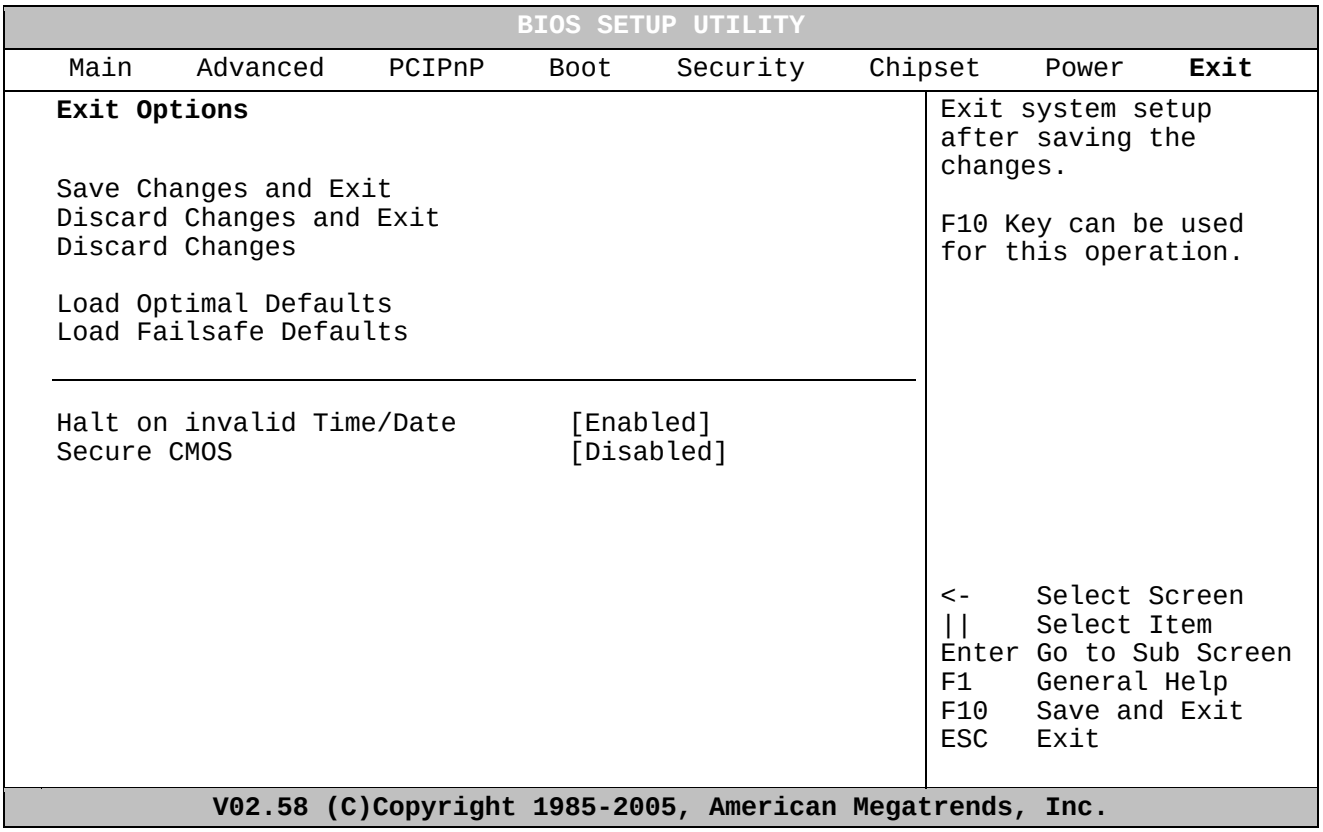
Feature	Options	Description
System Memory Frequency	100 MHz 133 MHz **Auto**	Controls the system meory frequency. If auto is selected it will be based on the SPD DIMM data.
Primary Video Device	Internal External PCI External AGP **Auto**	Select which graphics controller to use as the primary boot device.
Display Cache Window Size	32MB **64MB**	Select the size of the Graphics Local Memory Window.
Internal Graphic Scaling	**Auto** Disabled Enabled	Controls Video Scaling.
Output Device Sync/Non-sync	**Non-Synchronous** Synchronous	Select between synchronous or non-synchronous mode.
AGP Graphics Aperture Size	32MB **64MB**	Select Aperture Size
Backlight Signal Inversion	Disabled **Enabled**	Select the signal polarity
LCDVCC Voltage	**3.3V** 5V	Setup the LCD Voltage
LVDS	Panels	Chose the connected LVDS panel
DVI	**N/A**	Select the DVI connection

8.8 Power Menu



Feature	Options	Description
Power Management/APM	Disabled **Enabled**	Setup the SMI/APM support
Power Button Mode	**On/Off** Suspend	Select Power button functionality
Force Throttle	**Disabled** Enabled	Disable/Enable the Force to Thermal Throttle function.
THRM throttle Ratio	87.5% 75.0% 62.5% **50%** 37.5% 25% 12.5%	Select the duty cycle in throttle when the thermal override condition occurs. (Speed = 100% - N). Conditions can be defined in Hardware Health Configuration.
RTC Resume	Enabled **Disabled**	Let the board start up on a specific date and time
RTC Alarm Date	Every Day 1-31	Setup the date you want the board to start
RTC Alarm Time	HH:MM:SS	Setup the time you want the board to start
PME/WOL Enable	Enabled **Disabled**	Select PME to power on system with WOL function
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	When disabled the board can wake from S1 and S3, and when enabled it can also wake from S4 and S5.
S3-S5 Keyboard Hotkey	**Any key** Space Enter Sleep button	Setup the key that can wake up the board
AC Power Loss Restart	**Off** On Previous State	Select whether or not to restart the system after AC power loss: **Off** keeps the power off until the power button is pressed. **On** restores power to the computer. **Previous State** restores the previous power state before power loss occurred.

8.9 Exit Menu



Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	**Enabled** Disabled	Shall the BIOS halt and wait for a keypress when the cmos is corrupted
Secure CMOS	**Disabled** Enabled	Enable will store the current CMOS in the BIOS flash rom, this will maintain the settings even if the battery is failing

8.10 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

9. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on the 786LCD/mITX Driver CD or they can be downloaded from the homepage www.kontron-emea.com

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9.1 How to install SATA and RAID while installing Windows XP

Required HW:

IDE CD-ROM
Windows XP SP2 Installation CD.
SATA disk(s)
USB FDD

Required SW:

The file 786LCDmITX_Raid_Driver_Windows which can be downloaded from www.kontron-emea.com. The files shall be unzipped and the files (txt-file and doc-file are not needed) shall be copied to the Floppy Disk.

The file contains:

Readme.txt
SilSupp.cpl
SilSupp.vxd
SIEinAcc.sys
SI3112r.sys
SI3112r.inf
txtsetup.oem
si3112r.cat
Sil3x12A-Serial ATA (SATA) Windows RAID Driver.doc

Prepare target 786LCD/mITX board

Connect the Floppy Drive and Floppy Disk.
Connect CD-ROM drive and put in the Windows XP CD.
Connect the SATA Disk(s).

BIOS selection:

Exit>Load Optimized Default
Advanced>SATA/RAID Configuration [Enabled]
Boot>Boot Device Priority>1st Boot Device ["actual CD-rom drive"]
Exit>Save Changes and Exit (the next step of the process automatically starts.

Installation of XP

System will start but after a few seconds it will ask you to hit a key for booting on CD ... (hit a key)

Installation of the XP starts, but after a few seconds
it will ask you to press <F6> for installation of third part driver... (press the <F6> key).

After 1-2 minutes system will ask for installation drivers.
Press "S"
Select "Silicon Image Sil 3x12 SATARaid Controller for Windows XP/Server 2003" and press <enter>

Follow the guidelines to continue installing XP.

10. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.